ARM Cortex-M0+ 32-bit MCU, 24 KB Flash, 3 KB SRAM, 2xUART, I2C, SPI, Timers, ADC, 2xCOMP, 1.8-5.5V Datasheet

Features

- 48 MHz Cortex-M0+ 32-bit CPU
  Single-cycle multiplication instructions
- Up to 24 KB Flash and 3 KB SRAM
- Flexible power consumption management
  - Sleep,Stop,Deepstop multiple low-power modes
- Power detector: BOR
- Clock sources
  - Internal high-speed clock: 48MHz, full temperature variation within ±2%
  - Internal low-power, low-speed clock: 32 kHz
  - External clock input
- Up to 18 I/Os
  - All mappable on external interrupt vectors
  - Driving current up to 20 mA
- Timers
  - 1x16-bit advanced-control timer, can output 4 channels of PWM or 3 channels of complementary PWM, supporting dead-time insertion and break input
  - 1x 16-bit general-purpose timer, can output 4 channels of PWM or capture 2 channels of input signals, supporting hall-sensor
  - 1x 16-bit low-power timer, supporting wake-up from Deepstop and Stop mode
  - 1x 24-bit SysTick
  - 1x watchdogs: IWDG
- IRTIM supporting timer and UART connection for infrared control
- Communication interfaces
  - 1x SPI, with the maximum rate of 24 Mbps in master mode and 16 Mbps in slave mode
  - 2x UARTs
  - 1x I2C, slave mode, 1 Mbps Fm+
- 12-bit 1 Msps high-accuracy SAR ADC, supporting measure signals with high output impedance
  - 8 external channels
  - 1 internal channels for BGR reference voltage,can be used to evaluate the actual V_{DDA} voltage
- 2x low-power comparers, can be used in Deepstop and Stop mode
- CRC 16/32 calculation unit
- 96-bit unique ID
- Serial wire debug (SWD)
- Operating conditions: 1.8V~5.5V
- Operating temperature: -40 ℃~85 ℃, -40 ℃~105 ℃
- Packages: TSSOP20, QFN20, SOP16, SOP8

Declaration

The right to change the manual without notice to the user is reserved by CEC Huada Electronic Design Co., Ltd. Although we have reviewed the content of this manual, it is inevitable that it may still contain errors. As a result, we will periodically review the content of this manual and make necessary modification in the next release of the document. We recommend that you obtain the latest version from CEC Huada Electronic before finalizing your design.

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1 Introduction

The CIU32F003 security MCU is based on ARM Cortex-M0+ core. The maximum frequency is up to 48 MHz, equipping with up to 24K bytes Flash,3K bytes SRAM .It is available in multiple packages, including TSSOP20,QFN20,SOP16,SOP8. Abundant peripherals are built in, including 1Msps ADC, 2xlow-power comparer, 24Mbps SPI, 2x UART,I2C,multiple timers.

Application scenarios of CIU32F003 security MCUs:

- Lighting
- Electronic cigarettes
- Electric vehicle dashboards
- BMS, and other scenarios where 32-bit MCU replaces 8/16-bit

2 Product description

The CIU32F003 security MCU is equipped with up to 24 Kbytes of Flash and 3 Kbytes of SRAM, and other abundant peripherals. It is available in multiple packages, including TSSOP20, QFN20, SOP16, SOP8. The peripherals vary with the selected model and package form. For details, refer to the table below.

Table 2-1 CIU32F003 characteristics and peripherals

Peripheral		CIU32F003			
		F5P6	**F5U6**	**W5S6**	**J5S6**
Package		TSSOP20	QFN20	SOP16	SOP8
Flash(Kbytes)		24			
SRAM(Kbytes)		3			
CPU		Cortex-M0+ core			
		Maximum frequency 48MHz			
Timer	Advanced control Timer	1（16-bit）			
	General purpose Timer	1（16-bit）			
	LPTIM	1（16-bit）			
	PWM	8			4
	SysTick	1			
	IWDG	1			
Communication interfaces	UART	2			
	SPI	1			
	I2C	1			
	IRTIM	1			
CRC		√			
GPIOs		18	18	14	6
12-bit ADC		8 external channels +1 internal channel	8 external channels +1 internal channel	7 external channels +1 internal channel	4 external channels +1 internal channel
COMP		2			

3 Pin description

3.1 Pinouts

This chip is available in multiple packages, including TSSOP20,QFN20,SOP16,SOP8, etc. The pinout is shown in the figure below.

Figure 3-1 CIU32F003F5P6-TSSOP20 pinout

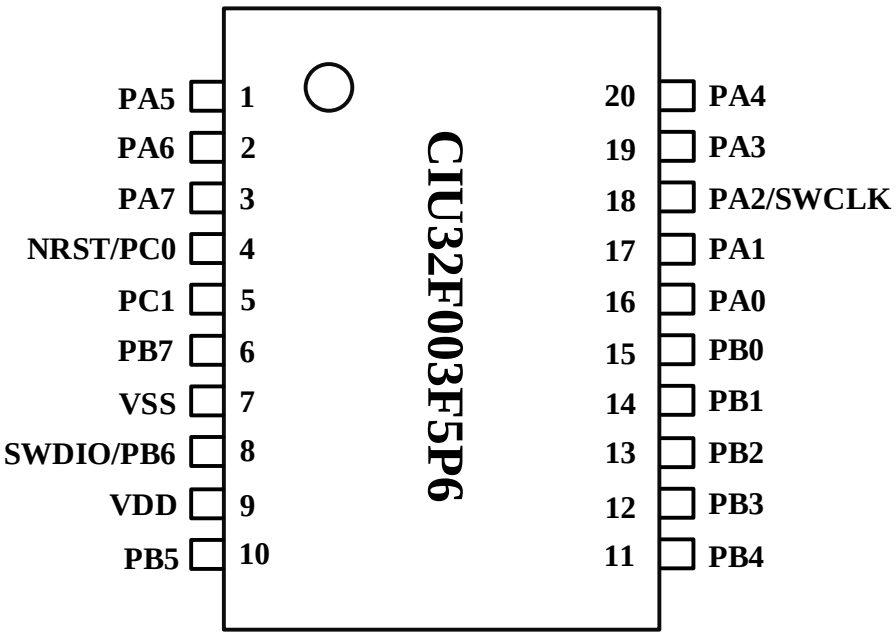


Figure 3-2 CIU32F003F5U6-QFN20 pinout

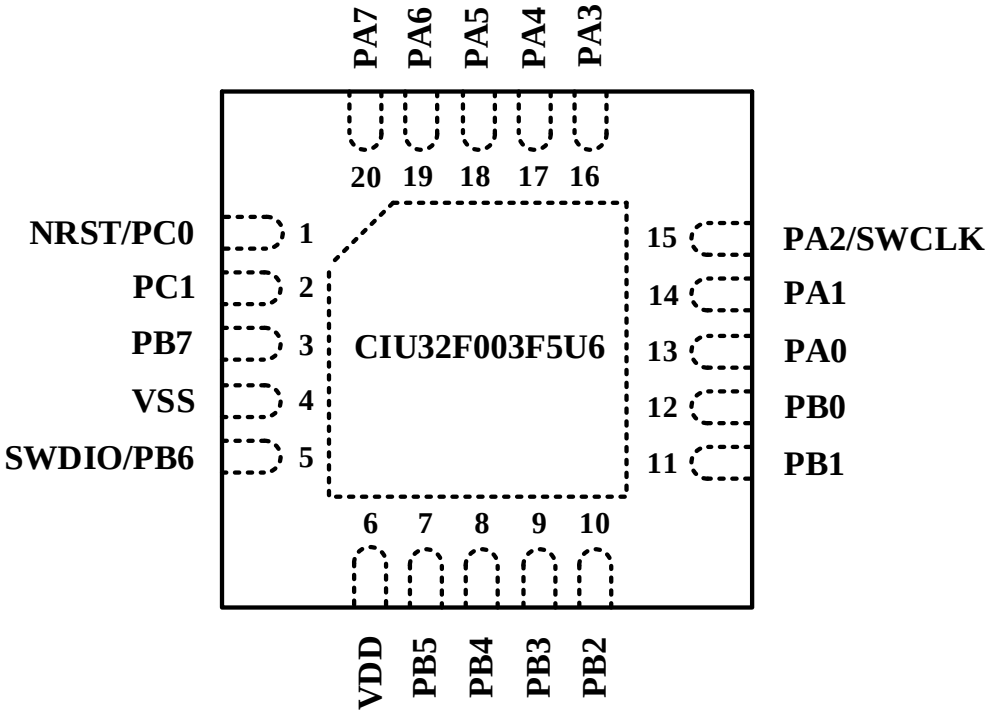


Figure 3-3 CIU32F003W5S6-SOP16 pinout

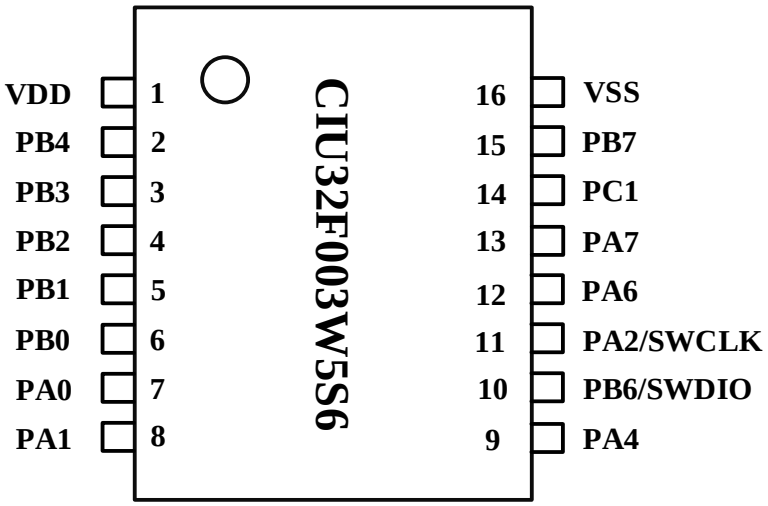
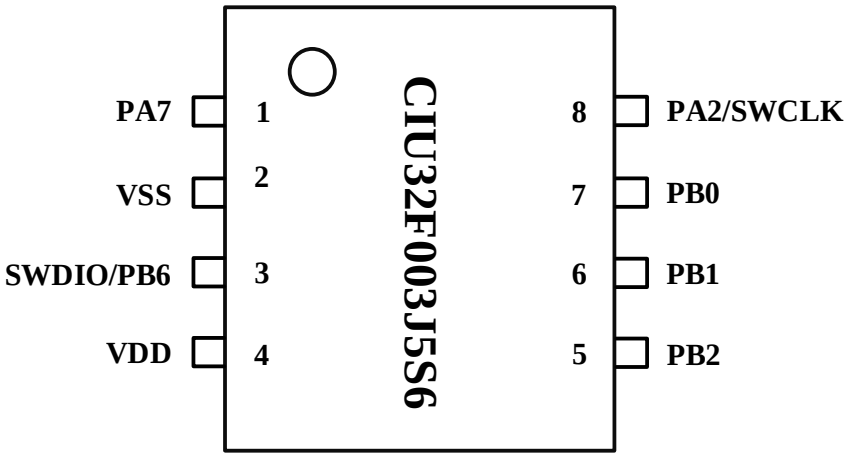


Figure 3-4 CIU32F003J5S6-SOP8 pinout



3.2 Pin definition

Table 3-1 Pin assignment and description

Pin No.				Pin name	Pin type	Additional functions	Alternate functions
TSSOP20	QFN20	SOP16	SOP8				
1	18	-	-	PA5	I/O	-	TIM1_CH2 TIM3_CH1 UART2_TX
2	19	12	-	PA6	I/O	ADC_IN3	SPI1_NSS UART1_TX TIM3_CH3 SPI1_SCK UART2_RX
3	20	13	1	PA7	I/O	ADC_IN4	SPI1_MOSI UART1_TX TIM3_CH2 UART1_RX MCO IR_OUT
4	1	-	-	PC0	I/O	NRST(1)	SWDIO UART1_TX
5	2	14	-	PC1	I/O	EXTCLK	SPI1_MISO TIM1_CH2 TIM3_CH1
6	3	15	-	PB7	I/O	-	SPI1_MOSI UART1_RX TIM1_CH1N TIM1_CH2N TIM1_CH4
7	4	16	2	VSS	G	-	-
8	5	10	3	PB6	I/O	ADC_IN6	SWDIO UART1_TX SPI1_MISO UART2_TX I2C1_SDA MCO
9	6	1	4	VDD	P	-	-
10	7	-	-	PB5	I/O	-	SPI1_NSS

							UART1_RX TIM1_CH3N TIM3_CH3
11	8	2	-	PB4	I/O	-	UART1_TX TIM1_BKIN TIM3_CH4 I2C1_SDA IR_OUT
12	9	3	-	PB3	I/O	ADC_IN5	TIM1_CH1N COMP1_OUT I2C1_SCL
13	10	4	5	PB2	I/O	-	SPI1_SCK TIM1_CH1 TIM1_CH1N TIM1_CH3 UART2_RX
14	11	5	6	PB1	I/O	ADC_IN0 COMP1_INM COMP1_INP	SPI1_NSS TIM1_CH1N TIM1_CH2N TIM1_CH4 MCO
15	12	6	7	PB0	I/O	ADC_IN7 COMP1_INP	SPI1_SCK UART1_TX TIM1_CH2 TIM3_CH1
16	13	7	-	PA0	I/O	-	SPI1_MOSI TIM1_CH1 TIM3_CH1 TIM1_CH2N TIM1_CH3N
17	14	8	-	PA1	I/O	-	SPI1_MISO TIM1_CH2 TIM1_CH3
18	15	11	8	PA2	I/O	-	SWCLK UART1_RX COMP1_OUT I2C1_SCL COMP2_OUT

19	16	-	-	PA3	I/O	ADC_IN1 COMP2_INP	UART1_TX TIM1_CH3N TIM3_CH3 UART2_RX
20	17	9	-	PA4	I/O	ADC_IN2 COMP2_INM COMP2_INP	UART1_RX TIM1_CH2N TIM3_CH2 UART2_TX

1. The function of PC0 is configured by the option bytes,The PC0 is used for NRST after reset.

Table 3-2 I/O alternate function remapping

PORT	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI1_MOSI	-	TIM1_CH1	TIM3_CH1	TIM1_CH2N	TIM1_CH3N	-	-
PA1	SPI1_MISO	-	TIM1_CH2	-	TIM1_CH3	-	-	-
PA2	SWCLK	UART1_RX	-	-	COMP1_OUT	-	I2C1_SCL	COMP2_OUT
PA3	-	UART1_TX	TIM1_CH3N	TIM3_CH3	-	UART2_RX	-	-
PA4	-	UART1_RX	TIM1_CH2N	TIM3_CH2	-	UART2_TX	-	-
PA5	-	-	TIM1_CH2	TIM3_CH1	-	UART2_TX	-	-
PA6	SPI1_NSS	UART1_TX	-	TIM3_CH3	SPI1_SCK	UART2_RX	-	-
PA7	SPI1_MOSI	UART1_TX	-	TIM3_CH2	-	UART1_RX	MCO	IR_OUT
PB0	SPI1_SCK	UART1_TX	TIM1_CH2	TIM3_CH1	-	-	-	-
PB1	SPI1_NSS	-	TIM1_CH1N	TIM1_CH2N	TIM1_CH4	-	MCO	-
PB2	SPI1_SCK	-	TIM1_CH1	TIM1_CH1N	TIM1_CH3	UART2_RX	-	-
PB3	-	-	TIM1_CH1N	-	COMP1_OUT	-	I2C1_SCL	-
PB4	-	UART1_TX	TIM1_BKIN	TIM3_CH4	-	-	I2C1_SDA	IR_OUT
PB5	SPI1_NSS	UART1_RX	TIM1_CH3N	TIM3_CH3	-	-	-	-

PORT	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB6	SWDIO	UART1_TX	-	-	SPI1_MISO	UART2_TX	I2C1_SDA	MCO
PB7	SPI1_MOSI	UART1_RX	TIM1_CH1N	TIM1_CH2N	TIM1_CH4	-	-	-
PC0	SWDIO	UART1_TX	-	-	-	-	-	-
PC1	SPI1_MISO	-	TIM1_CH2	TIM3_CH1	-	-	-	-

4 Electrical characteristics

4.1 Test conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

TBD indicates data to be defined.

4.2 Minimum and maximum values

Unless otherwise specified, the values are obtained through tests on 100% products in the production line at the temperature of T_A=25℃ and T_A=$T_A$max (where $T_A$max matches with the selected temperature range). All the minimum and maximum values can be guaranteed under the worst ambient temperature, power supply voltage, and clock conditions.

The data obtained through comprehensive assessment, designing simulation, and/or process characteristics as described in the notes below each table is not tested in the production line. On the basis of comprehensive assessment, the minimum and maximum values are normal distribution of average values multiplied or divided by three times after sample tests (mean ±3σ).

4.3 Typical values

Unless otherwise specified, typical values are based on T_A=25℃ and V_{DD}=3.3V (1.8V≤V_{DD}≤5.5V).

4.4 Absolute maximum ratings

Stresses on the device above the values listed in the table below (voltage, current, and temperature) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage characteristics(1)

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External supply voltage	-0.3	5.8	V
V_{DDA}-V_{SS}	External analog supply voltage	-0.3	5.8	V
V_{IN}	Pin input voltage(2)	V_{SS}-0.3	V_{DD}+0.3	V

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies in the permitted range.

2. V_{IN} maximum values must always be followed. For the maximum allowed injected current values, refer to *Table: Current characteristics*.

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
$I_{VDD/VDDA}$	Current into the V_{DD}/V_{DDA} power pin(1)	100	mA
$I_{VSS/VSSA}$	Current out of the V_{SS}/V_{SSA} ground pin(1)	100	
$I_{IO(PIN)}$ (2)	Output current sunk by I/O and control pins	20	
	Output current sourced by I/O and control pins	20	
$I_{INJ(PIN)}$(3)	I/O injected current	-5/5	
$\Sigma\|I_{INJ(PIN)}\|$(4)	Total injected current (sum of all I/O and control pins)	25	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies in the permitted range.
2. The output sink current and pull current of the I/O and control pins are the maximum currents at TA=25 ℃ and V_{DD}=5V and at V_{OL}=V_{SS}+0.6V and V_{OH}=V_{DD}-0.6V, respectively.
3. The positive injected current is generated when $V_{IN} > V_{DD}$. When $V_{IN} < V_{SS}$, the negative injected current generated. Injected current should be limited to be within $I_{INJ(PIN)}$.
4. The maximum value of $\Sigma|I_{INJ(PIN)}|$ equals the sum of the absolute values of the positive injected current and the negative injected current (instantaneous values) when injected currents are present on multiple inputs at the same time.

Table 4-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	℃
T_J	Maximum junction temperature	105	℃

4.5 Operating conditions

4.5.1 General operating conditions

Table 4-4 General operating conditions

Symbol	Description	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	48	
f_{PCLK2}	Internal APB2 clock frequency	-	0	48	

Symbol	Description	Condition	Min	Max	Unit
V_{DD}	Digital supply voltage	-	1.8	5.5	V
V_{DDA}	Analog supply voltage	-	1.8	5.5	
T_A	Ambient temperature	-	-40	85	℃
T_J	Junction temperature	-	-40	105	℃

4.5.2 Operating conditions at power-up/power-down

Table 4-5 Operating conditions at power-up/power-down

Symbol	Description	Condition	Min	Max	Unit
t_{VDD}	V_{DD} slew rate	V_{DD} rising	0	∞	μs/V
		V_{DD} falling	60	∞	

4.5.3 Embedded resets and power control block characteristics

Table 4-6 Embedded resets and power control block

Symbol	Description	Condition	Min(1)	Typ(2)	Max(1)	Unit
V_{POR}	Power-on reset threshold	-	-	1.66	-	V
V_{PDR}	Power-down reset threshold	-	-	1.56	-	
V_{BOR0}	Brownout reset threshold 0	V_{DD} rising	-	1.99	-	
		V_{DD} falling	-	1.90	-	
V_{BOR1}	Brownout reset threshold 1	V_{DD} rising	-	2.39	-	
		V_{DD} falling	-	2.30	-	
V_{BOR2}	Brownout reset threshold 2	V_{DD} rising	-	2.79	-	
		V_{DD} falling	-	2.70	-	
V_{BOR3}	Brownout reset threshold 3	V_{DD} rising	-	2.91	-	
		V_{DD} falling	-	2.79	-	
V_{hyst_POR}	Hysteresis of V_{POR}		-	100	-	mV
V_{hyst_BOR}	Hysteresis of V_{BORx}		-	100	-	mV
$I_{DD(BOR)}$	BOR power consumption		-	0.3	-	μA

4.5.4 Embedded voltage reference

Table 4-7 Embedded voltage reference

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{BGR}	Embedded reference voltage	-40 ℃~85 ℃	0.784	0.8	0.816	V
t_{SAMP} (1) (2)	Sampling time when reading the internal channel V_{BGR}	-	12	-	-	μs
t_{ADC_BUF}(1) (2)	Start time of the ADC internal channel V_{BGR} buffer	-	-	22	60	μs

1. Guaranteed by design. Not tested in production.
2. Wait for the startup stabilization time t_{ADC_BUF} to enable the ADC internal channel V_{BGR}. The sampling time for ADC to measure the internal channel V_{BGR} should be at least t_{SAMP}.

4.5.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is placed under the following conditions:

- All I/O pins are in the analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (0 wait cycles for 0~24 MHz, 1 wait cycle for 24~48 MHz).
- When the peripherals are enabled: $f_{PCLK} = f_{HCLK}$.

Table 4-8 Current consumption in Run mode

Symbol	Descri -ption	Condition(1)				Typ	Unit
		Mode	Clock source	f_{HCLK}	Operating area		
$I_{DD(Run)}$	Supply current	All peripherals disabled; the CPU	RCH clock source	48MHz	Flash	1.52	mA
			RCH clock source,	16MHz		0.94	

Symbol	Descri -ption	Condition(1)				Typ	Unit
		Mode	Clock source	f_{HCLK}	Operating area		
	(Run mode)	get instructions from Flash; While (1)	divided by 3				
			RCH clock source, divided by 6	8MHz		0.9	
		All peripherals enabled; the CPU get instructions from Flash; While (1)	RCH clock source	48MHz	Flash	2.12	

1. Test conditions: V_{DD} = 3.3V, T_A=25 ℃.

Table 4-9 Current consumption in Sleep mode

Symbol	Description	Condition(1)				Typ	Unit
		Mode	Clock source	f_{HCLK}	Operating area		
$I_{DD(Sleep)}$	Supply current (Sleep mode)	All peripherals disabled	RCL clock source	32KHz	Flash	221	μA
			RCH clock source	48MHz		670	
			RCH clock source, divided by 6	8MHz		480	

1. Test conditions: V_{DD} = 3.3V, T_A=25 ℃.

Table 4-10 Current consumption in Stop mode

Symbol	Description	Condition(1)		Typ	Unit
		Mode	V_{DD}		
$I_{DD(Stop)}$	Supply current (Stop mode)	All peripherals disabled	3.3V	220	μA

1. Test conditions: T_A=25 ℃.

Table 4-11 Current consumption in Deepstop mode

Symbol	Description	Condition(1)		Typ	Unit
		Mode	V_{DD}		
$I_{DD(Deepstop)}$	Supply current (Deepstop mode)	All peripherals disabled	3.3V	5.23	μA

1. Test conditions: T_A=25 ℃.

4.5.6 Wakeup time from low-power modes

The wakeup times are the latency between the event and the execution of the first user instruction.

Table 4-12 Wakeup time from low-power modes(1)

Symbol	Description	Condition	Typ	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode	Transiting to Run-mode execution in Flash memory: HCLK = RCH = 48MHz	12	CPU cycles
t_{WUSTOP}	Wakeup time from Stop mode	Transiting to Run-mode execution in Flash memory	2.91	μs
$t_{WUDEEPSTOP}$	Wakeup time from DeepStop mode	Transiting to Run-mode execution in Flash memory	12.68	
		Transiting to Run-mode execution in SRAM memory	5.75	

1. Derived from comprehensive assessment.

4.5.7 External clock source characteristics

External clock input directly.

Table 4-13 External clock characteristics (1)

Symbol	Description	Min	Typ	Max	Unit
F_{EXTCLK}	External High-speed external clock (EXTCLK) frequency	-	-	24	MHz
$V_{EXTCLKH}$	EXTCLK_IN input pin high level voltage	$0.7V_{DD}$	-	V_{DD}	V
$V_{EXTCLKL}$	EXTCLK_IN input pin low level voltage	V_{SS}	-	$0.3V_{DD}$	

1. Derived from comprehensive assessment.

4.5.8 Internal clock source characteristics

RCH（16MHz）

Table 4-14 Internal RCH oscillator characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{RCH}	RCH frequency	-	-	48	-	MHz
$\Delta Temp_{(RCH)}$	RCH frequency drift over temperature	V_{DD}=1.8V~5.5V T_A= 0 ℃ ~ 60 ℃	-1	-	1	%
		V_{DD}=1.8V~5.5V	-2	-	2	

Symbol	Description	Condition	Min	Typ	Max	Unit
		T_A= -40 ℃ ~ 85 ℃				
$I_{DD(RCH)}$ (1)	RCH oscillator power consumption	-	-	225	-	μA
$Duty_{(RCH)}$ (2)	Duty cycle	-	45	-	55	%
$t_{SU\ (RCH)}$ (1)	RCH startup time	-	-	1	-	μs
$t_{STAB(RCH)}$ (1)	RCH stabilization time	-	-	0.12	-	μs

1. Derived from comprehensive assessment.
2. Guaranteed by design. Not tested in production.

RCL（32KHz）

Table 4-15 Internal RCL oscillator characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{RCL}	RCL frequency	-	-	32	-	KHz
$\Delta Temp_{(RCL)}$	RCL frequency drift over temperature	V_{DD}=1.8V~5.5V T_A=25°C	-5	-	5	%
		V_{DD}=1.8V~5.5V T_A= -40°C ~ 85°C	-15	-	15	
$I_{DD(RCL)}$ (1)	RCL oscillator power consumption	-	-	125	-	nA
$Duty_{(RCL)}$ (2)	Duty cycle	-	-	50	-	%
$t_{SU(RCL)} + t_{STAB(RCL)}$ (1)	Startup stabilization time	-	-	70	-	μs

1. Derived from comprehensive assessment.
2. Guaranteed by design. Not tested in production.

4.5.9 Flash memory characteristics

Table 4-16 Flash memory characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
t_{PROG}	Word programming time	-	-	50	-	μs
t_{ERASE}	Erase time	Page erase	-	2.5	-	ms
		Mass erase	-	35	-	ms
EC_{Flash}	Endurance	T_A= -40 ℃~85 ℃	100000	-	-	cycles
RET_{Flash}	Data retention	T_A= 85 ℃	25	-	-	years

1. Derived from comprehensive assessment.

4.5.10 EMC characteristics

Table 4-17 EMC characteristics(1)

Symbol	Description	Condition	Level/type
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	T_A = 25 ℃ According to IEC 61000-4-2	4A
V_{EFTB}	Fast transient voltage burst limits to be applied on V_{DD} and V_{SS} pin to induce a functional disturbance	T_A = 25 ℃ According to IEC 61000-4-4	5A

1. Derived from comprehensive assessment.

4.5.11 ESD characteristics

Table 4-18 ESD characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Human body model	T_A = 25 ℃ According to ESDA/JEDEC JS-001-2017	-	±4000	-	V
$V_{ESD(CDM)}$	Charge device model	T_A = 25 ℃ According to ESDA/JEDEC JS-002-2018	-	±2000	-	

1. Derived from comprehensive assessment.

Table 4-19 Latch-up characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
$I_{Latch-up}$	Latch-up current	T_A = 25 ℃ According to JEDEC78E	-	±300	-	mA

1. Derived from comprehensive assessment.

4.5.12 I/O port characteristics

Table 4-20 Input characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{IL}(1)	Input low level voltage	-	-	-	$0.3V_{DD}$	V
V_{IH}(1)	Input high level voltage	-	$0.7V_{DD}$	-	-	
V_{hys}(1)	Schmitt trigger voltage hysteresis	-	-	320	-	mV

Symbol	Description	Condition	Min	Typ	Max	Unit
I_{lkg}(1)	Input leakage current	-	-	9.6	-	nA
R_{PU}(2)	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	27	48	80	kΩ
R_{PD}(2)	Weak pull-down equivalent resistor	$V_{IN} = V_{DD}$	27	47	75	kΩ
C_{IO}(2)	I/O pin capacitance	-	-	1.72	-	pF

1. Derived from comprehensive assessment.
2. Guaranteed by design. Not tested in production.

Table 4-21 Output characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Uint
V_{OL}(2)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 5V	-	0.6	-	V
		$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V	-	0.32	-	
		$\|I_{IO}\|$ = 12mA V_{DD} = 3.3V	-	0.5	-	
V_{OH}(3)	Output high level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 5V	-	V_{DD}-0.6	-	
		$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V	-	V_{DD}-0.32	-	
		$\|I_{IO}\|$ = 12mA V_{DD} = 3.3V	-	V_{DD}-0.5	-	

1. Derived from comprehensive assessment.
2. The I_{IO} sink current must follow the absolute maximum ratings listed in *Table: Current characteristics*, and the total current of I_{IO} (I/O port and control pin) shall not exceed $I_{VSS/VSSA}$.
3. The I_{IO} pull current must follow the absolute maximum ratings listed in *Table: Current characteristics*, and the total current of I_{IO} (I/O port and control pin) shall not exceed $I_{VDD/VDDA}$.

Table 4-22 AC characteristics(1)

Symbol	Description	Condition	Min	Max	Uint
f_{MAX}	Maximum output frequency	C=50pF ， 1.8V≤V_{DD}＜2.7V	-	10	MHz
		C=50pF， 2.7V≤V_{DD}≤5.5V	-	20	
		C=30pF ， 1.8V≤V_{DD}＜2.7V		16	
		C=30pF ， 2.7V≤V_{DD}≤5.5V	-	32	
T_r	Rise time	C=50pF ， 1.8V≤V_{DD}＜2.7V	-	24.71	ns
		C=50pF ， 2.7V≤V_{DD}≤5.5V	-	14.81	

Symbol	Description	Condition	Min	Max	Uint
		C=30pF ， 1.8V≤V_{DD}＜2.7V	-	16.72	
		C=30pF ， 2.7V≤V_{DD}≤5.5V	-	10.07	
T_f	Fall time	C=50pF ， 1.8V≤V_{DD}＜2.7V	-	27.82	ns
		C=50pF ， 2.7V≤V_{DD}≤5.5V	-	17.15	
		C=30pF ， 1.8V≤V_{DD}＜2.7V	-	18.37	
		C=30pF ， 2.7V≤V_{DD}≤5.5V	-	11.25	

1. Guaranteed by design. Not tested in production.

4.5.13 NRST input characteristics

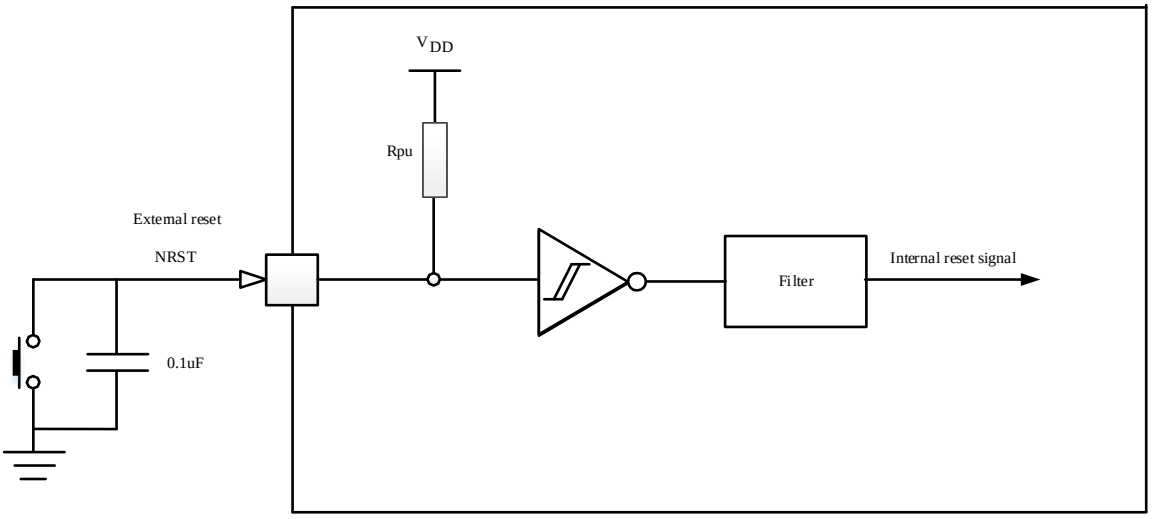
The NRST pin is connected to a permanent internal pull-up resistor. Therefore, it is not necessary to connect to an external pull-up resistor.

Table 4-23 NRST input characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
$V_{IL\ (NRST)}$	Input low-level voltage	-	-	-	0.3V_{DD}	V
$V_{IH\ (NRST)}$	Input high-level voltage	-	0.7V_{DD}	-	-	
$V_{hys\ (NRST)}$	Schmitt trigger voltage hysteresis	-	-	320	-	mV
R_{PU}	Pull-up equivalent resistor	V_{IN}=V_{SS}	6	10	18	kΩ
$T_{(NRST)}$ (2)	Filtered pulse	1.8V≤V_{DD}≤5.5V	500			μs

1. Guaranteed by design. Not tested in production.
2. The low-level signal on the NRST pin must be greater than 500 μs to reset the chip.

Figure 4-1 Recommended circuit for the NRST pin



1. The reset circuit can protect the MCU to avoid resets caused by noise interference.
2. The user must ensure that the electrical level on the NRST pin can be reduced to below the V_{IL} maximum level listed in the table of I/O input characteristics; otherwise, no reset is executed.
3. The external capacitor on NRST pin must be placed as close as possible to the device.

4.5.14 ADC characteristics

Table 4-24 ADC characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	5.5	V
V_{REF_ADC}	Reference voltage	-	1.8	-	V_{DDA}	V
f_{ADC_CK}	ADC clock frequency	2.2V＜V_{DDA}≤5.5V	0.3	-	16	MHz
		1.8V≤V_{DDA}≤2.2V	0.3	-	8	
f_S	Sampling rate	12 bits	-	-	1	Msps
V_{AIN}	Conversion voltage range	-	V_{SSA}	-	V_{DDA}	V
R_S	Input switch equivalent impedance	-	-	0.26	4.2	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	8	-	pF
t_{STAB}	ADC power-up time	-	-	-	1	μs
t_{CAL}	Calibration time	-	130	-	-	$1/f_{ADC\_CK}$
t_{SAMP}	Sampling time	-	3	-	1919	$1/f_{ADC\_CK}$
t_{CONV}	Total conversion time (including sampling time)	-	t_{SAMP} + 13			$1/f_{ADC\_CK}$

Symbol	Description	Condition	Min	Typ	Max	Unit
I_{DDA} (2)	ADC consumption	fs = 1Msps	-	320	-	μA

1. Guaranteed by design. Not tested in production.
2. Derived from comprehensive assessment.

Table 4-25 Sampling time and input signal impedance(1) (2)

Resolution	Sampling cycle (16 MHz)	Sampling time (16 MHz) (μs)	Maximum input impedance R_{AIN} (kΩ)
12bits	3	0.188	2.6
	7	0.438	4.6
	12	0.75	10.5
	19	1.188	23
	39	2.438	31
	79	4.938	40
	119	7.438	50
	159	9.938	67
	239	14.938	84
	319	19.938	124
	479	29.938	182
	639	39.938	223
	959	59.938	320
	1279	79.938	645
	1919	119.938	850

1. Derived from comprehensive assessment.
2. When using resistor voltage division to adjust the input signal voltage range, it is advisable to choose small resistance values while meeting power consumption requirements, in order to minimize the input signal impedance.

Table 4-26 ADC accuracy(1) (2)

Symbol	Description	Condition	Min	Typ	Max	Unit
DNL	Differential nonlinear error	$V_{DDA} = V_{REF\_ADC}$ = 3.3 V; fs= 1 Msps; T_A = 25 °C	-1	-	1.5	LSB
INL	Integral nonlinear error		-3	-	3	LSB
SNR	Signal-to-noise ratio	$V_{DDA} = V_{REF\_ADC}$ = 3.3 V; fs= 1 Msps; f_{IN}=1KHz;	-	63	-	dB
SINAD	Signal-to-noise and		-	61	-	dB

Symbol	Description	Condition	Min	Typ	Max	Unit
	distortion ratio	T_A = 25 °C				
THD	Total harmonic distortion		-	-65	-	dB
ENOB	Effective number of bits		-	9.8	-	bit

1. Derived from comprehensive assessment.
2. To further improve the acquisition accuracy, the factory-stored compensation values can be used to compensate the calibration coefficients. Please refer to the《RM1007_CIU32F003x5 Reference manual》for usage instructions.

4.5.15 COMP characteristics

Table 4-27 COMP characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
$V_{DDA(COMP)}$	Analog supply voltage	-	1.8	-	5.5	V
V_{IN}	COMP Input voltage	-	0	-	V_{DDA}-1.1	V
t_{START}	Startup time	-	-	0.11	0.44	μs
V_{offset}(2)	Offset voltage	-	-6.8	4.3	7.3	mV
V_{hys}	Hysteresis	-	-	30	-	mV
t_D	Propagation delay	-	-	0.14	-	μs
I_{COMP}	Static power consumption	Output high	-	6.43	-	μA
		Output low	-	3.85	-	μA
I_{DAC}	16-level voltage divider	-	-	9.62	-	μA

1. Derived from comprehensive assessment.
2. Guaranteed by design. Not tested in production.

4.5.16 SPI characteristics

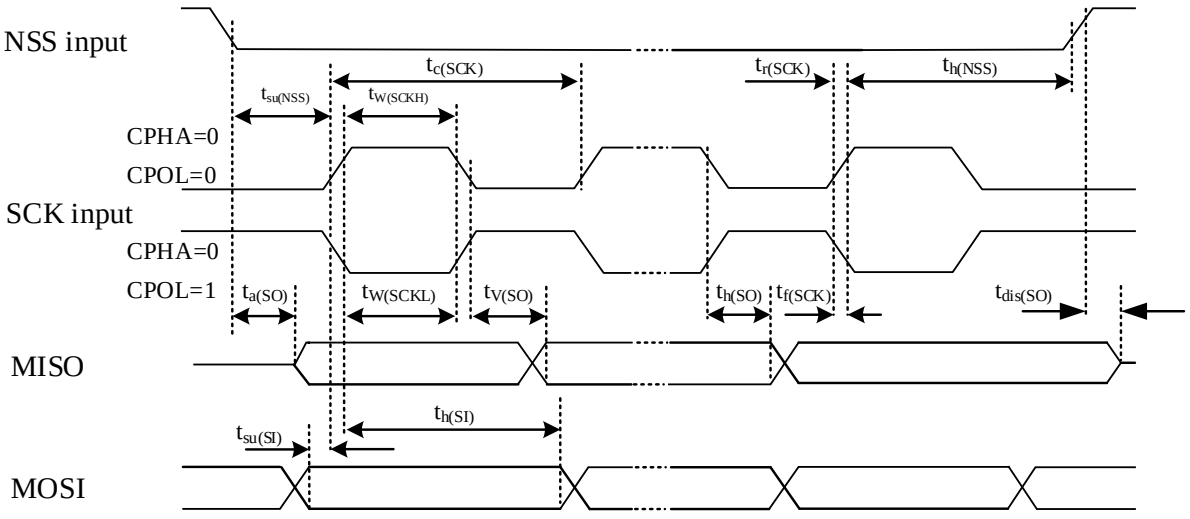
Table 4-28 SPI characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode	-	-	24	MHz
		Slave mode	-	-	16	MHz
$t_{SU(NSS)}$	NSS setup time	Slave mode	4.35	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	3.02	-	-	ns

Symbol	Description	Condition	Min	Typ	Max	Unit
$t_{W(SCKH)}$	SCK high time	Master mode	$T_{SCK}/2-1$	$T_{SCK}/2$	$T_{SCK}/2+1$	ns
$t_{W(SCKL)}$	SCK low time	Master mode	$T_{SCK}/2-1$	$T_{SCK}/2$	$T_{SCK}/2+1$	ns
$t_{SU(MI)}$	Data input setup time	Master mode	-	-	4.09	ns
$t_{SU(SI)}$		Slave mode	1.98	-	-	ns
$t_{h(MI)}$	Data input hold time	Master mode	0	-	-	ns
$t_{h(SI)}$		Slave mode	9.7	-	-	ns
$t_{V(MO)}$	Data output valid time	Master mode	-	-	2.94	ns
$t_{V(SO)}$		Slave mode	-	-	20.97	ns
$t_{h(MO)}$	Data output hold time	Master mode	2.42	-	-	ns
$t_{h(SO)}$		Slave mode	22.38	-	-	ns

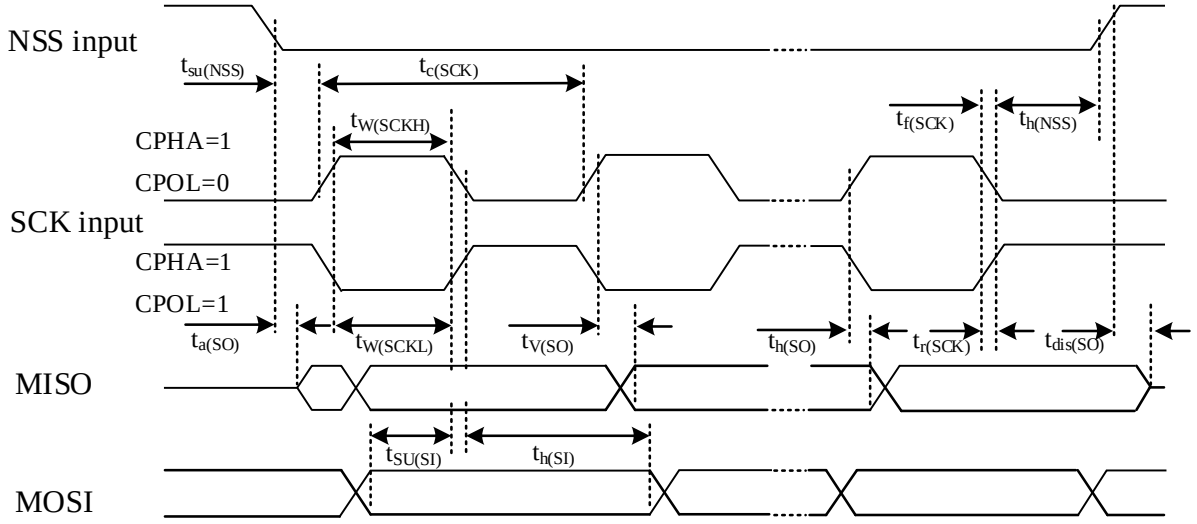
1. Guaranteed by design. Not tested in production.

Figure 4-2 SPI timing diagram - slave mode (CPHA = 0)(1)



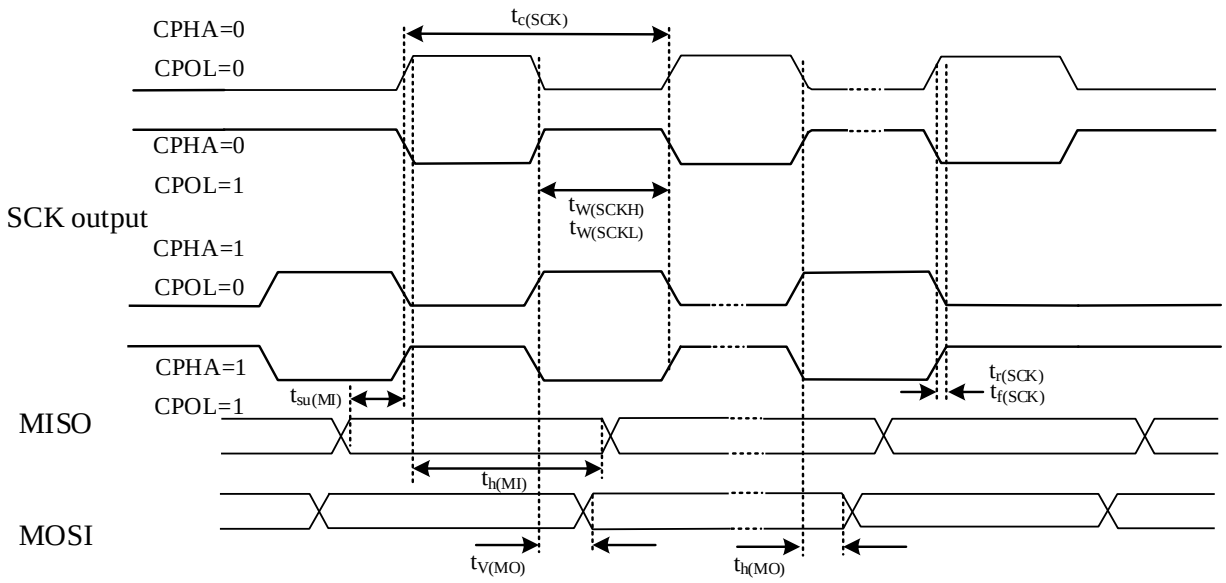
1. Measurement points are done at levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 4-3 SPI timing diagram - slave mode (CPHA = 1)(1)



1. Measurement points are done at levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 4-4 SPI timing diagram - master mode(1)



1. Measurement points are done at levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5 Package information

CIU32F003 offers TSSOP20（6.5 x 4.4 x 1.0 - 0.65mm）、QFN20（3 x 3 x 0.55 - 0.4mm）、SOP16（9.9 x 3.9 x 1.5 - 1.27mm）、SOP8（4.9 x 3.9 x 1.4 - 1.27mm）and multiple packages. It complies with the JEDEC standard. The package dimension and size information are described in this chapter.

5.1 TSSOP20 package information

Figure 6-1 TSSOP20 (6.5 x 4.4 x 1.0 - 0.65mm) package outline

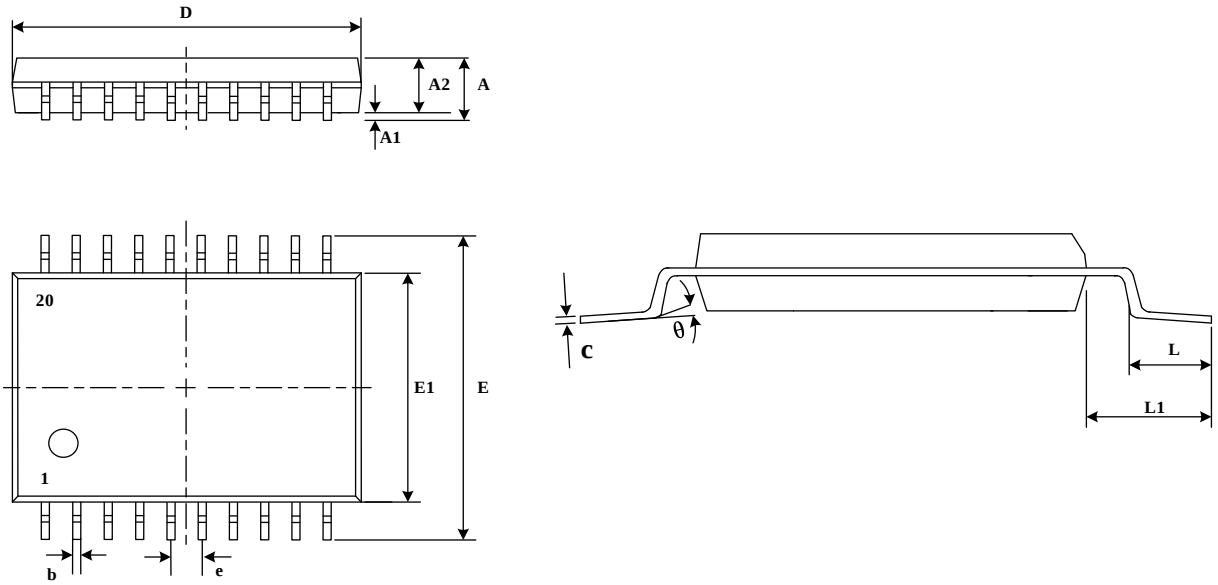


Table 5-1 TSSOP20 (6.5 x 4.4 x 1.0 - 0.65 mm) package outline dimension data

Symbol	Min	Typ	Max
A	-	-	1.20
A1	0.05	0.10	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.13	-	0.17
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75

Symbol	Min	Typ	Max
L1	0.85	1.00	1.15
θ	0	-	8°

5.2 QFN20 package information

Figure 6-2 QFN20 (3 x 3 x 0.55 - 0.4mm) package outline

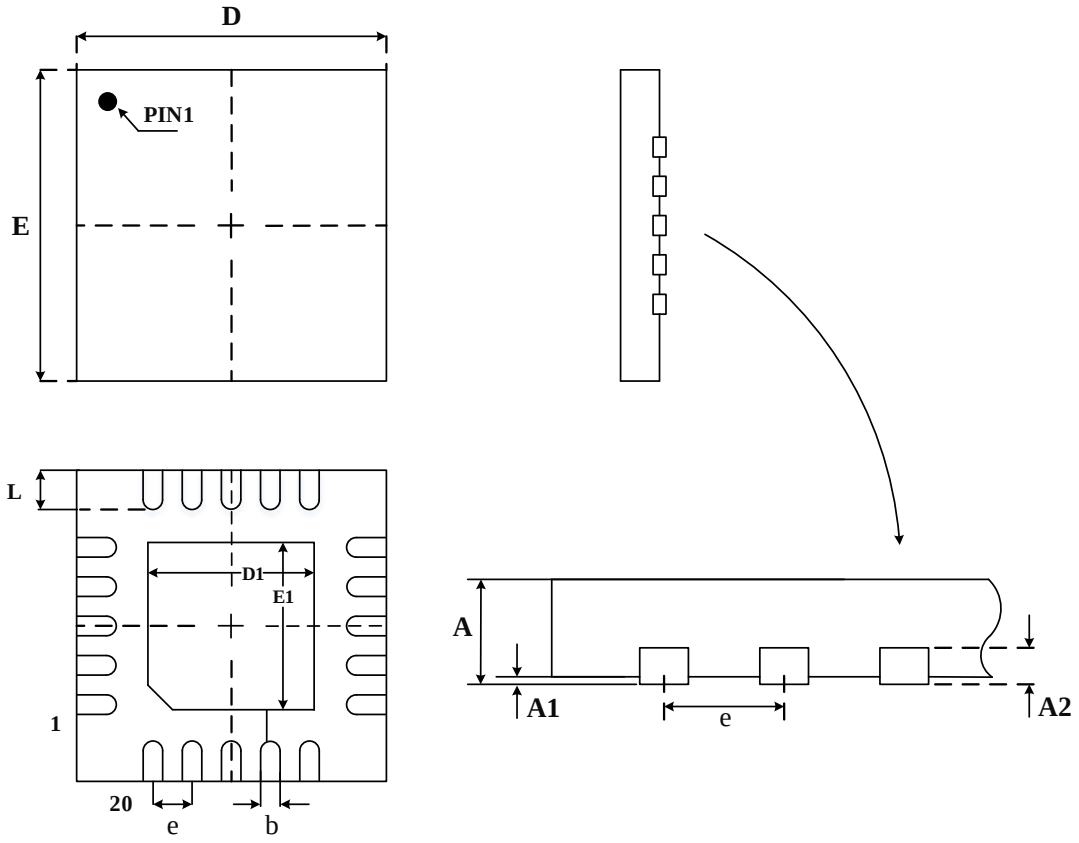


Table 5-2 QFN20(3 x 3 x 0.55 - 0.4 mm) package outline dimension data

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2	0.152REF		
b	0.15	0.20	0.25
D	3.00BSC		
E	3.00BSC		
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e	0.40BSC		

Symbol	Min	Typ	Max
L	0.25	0.30	0.35

5.3 SOP16 package information

Figure 5-3 SOP16(9.9 x 3.9 x 1.5 - 1.27mm) package outline

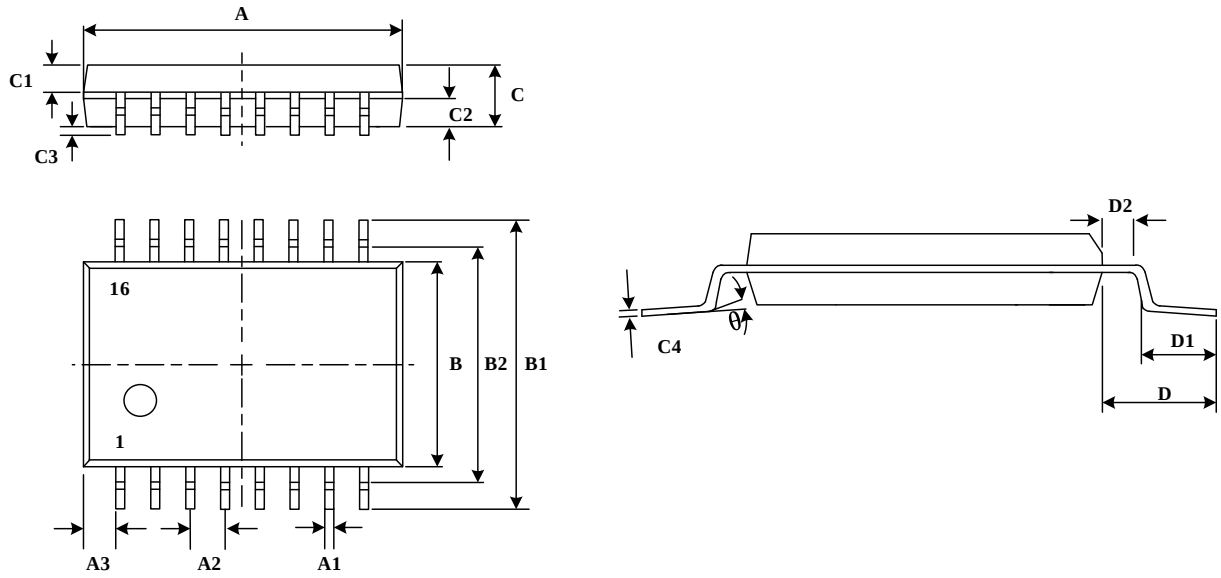


Table 5-3 SOP16(9.9 x 3.9 x 1.5 - 1.27 mm) package outline dimension data

Symbol	Min	Typ	Max
A	9.800	-	10.050
A1	0.350	-	0.456
A2	1.27 BSC		
A3	0.302 BSC		
B	3.850	-	3.950
B1	5.800	-	6.200
B2	5.00 BSC		
C	1.350	-	1.600
C1	0.550	-	0.750
C2	0.540	-	0.640
C3	0.050	-	0.250
C4	0.180	-	0.250
D	1.05BSC		
D1	0.400	-	0.800

Symbol	Min	Typ	Max
D2	0.150	-	0.250
θ	0	-	8°

5.4 SOP8 package information

Figure 5-4 SOP8 (4.9 x 3.9 x 1.4 - 1.27mm) package outline

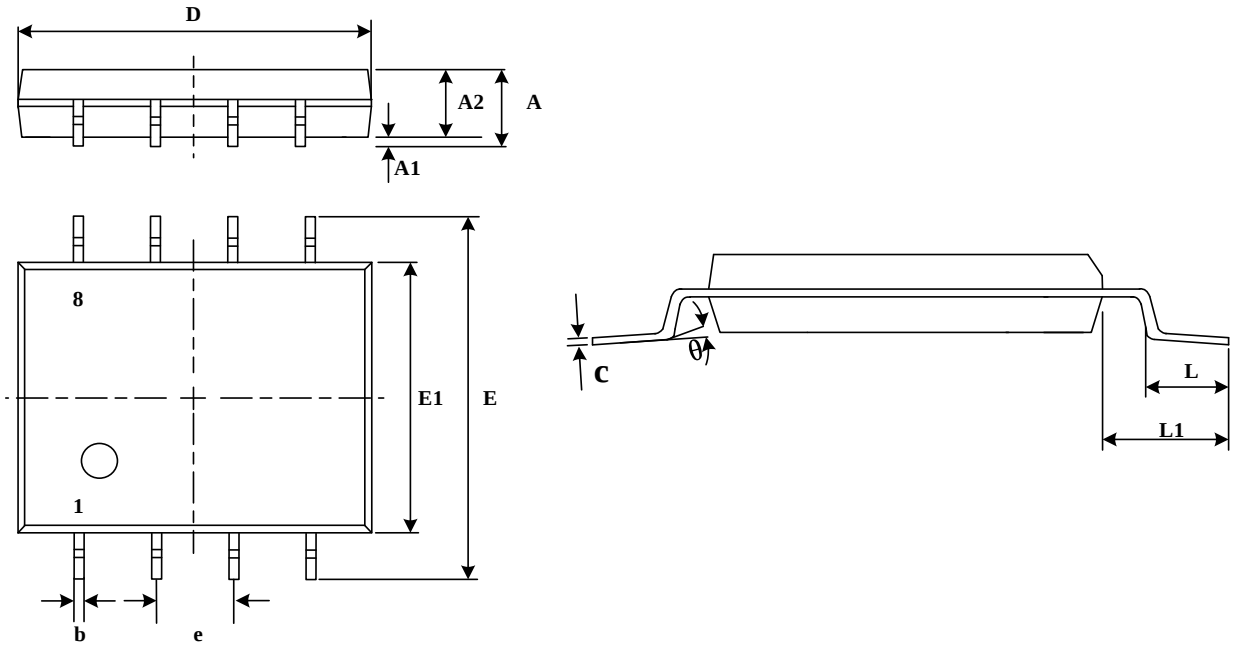


Table 5-4 SOP8 (4.9 x 3.9 x 1.4 - 1.27 mm) package outline dimension data

Symbol	Min	Typ	Max
A	-	-	1.750
A1	0.000	0.175	0.250
A2	1.250	1.400	1.550
b	0.310	-	0.500
c	0.100	-	0.250
D	4.700	-	5.100
E	5.800	6.000	6.200
E1	3.800	-	4.000
e	1.270BSC		
L	0.400	-	1.000
L1	1.100REF		
θ	0	-	8°

5.5 Silk screen description

The PIN1 identifier location and topside marking information on each package for the CIU32F003 security MCU are as follows:

Figure 5-5 TSSOP20/SOP16 silk screen information description

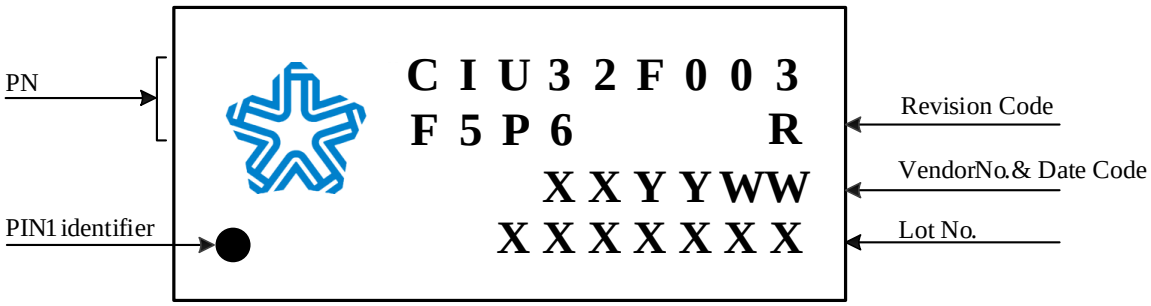


Figure 5-6 SOP8 silk screen information description

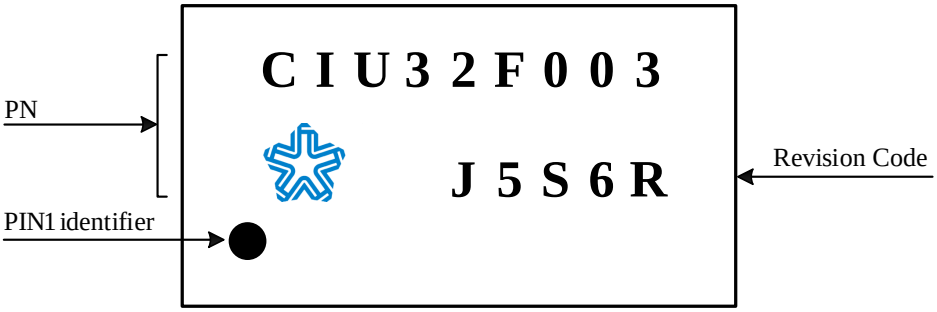
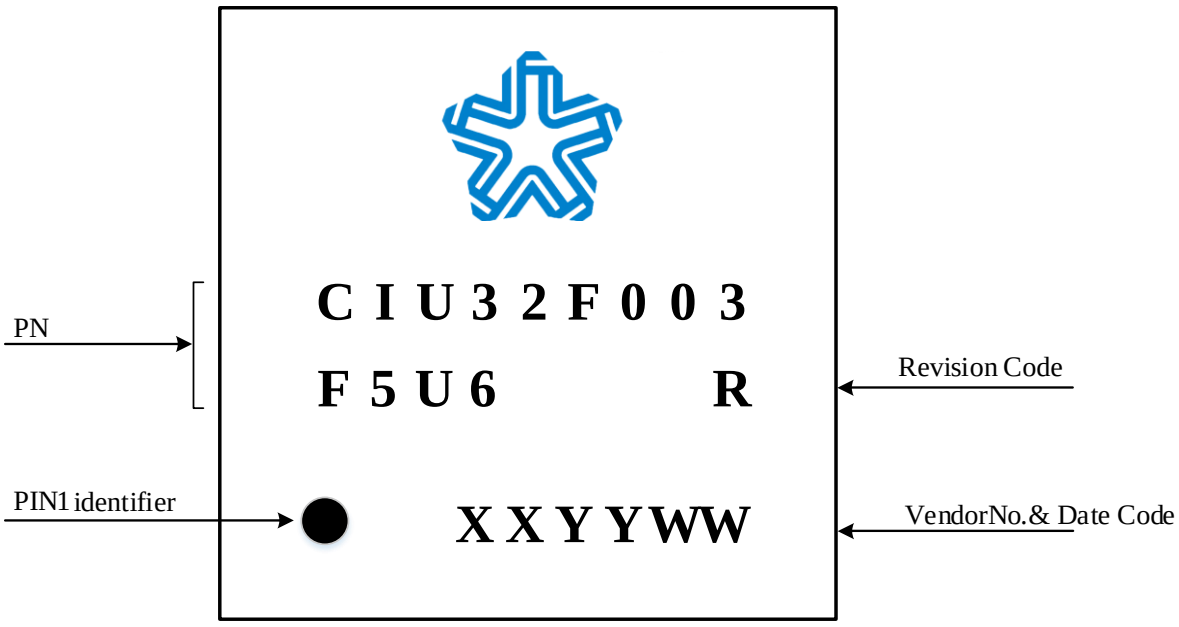


Figure 5-7 QFN20 silk screen information description



6 Ordering information

CIU 32 F 0 03 F 5 U 6 xx

CPU bit width

32：32bit

Product type

F：General-purpose

Core

0：Cortex-M0+

Device subfamily

03：CIU32F003

Pin count

J： 8Pin
W：16Pin
F： 20Pin

Flash memory size

5：24K

Package type

S：SOP
P：TSSOP
U：QFN

Temperature range

6：-40 ~ 85℃
7：-40 ~ 105℃

Packing form

TR：tape and reel packing
TU：tube packing

7 Revision history

Table 7-1 Revision history

Date	Revision	Changes
2024-4-18	V1.0	Initial release
2024-10-18	V1.1	Revised relevant content in Electrical characteristics
2024-11-18	V1.2	1、Corrected relevant content in EMC,ADC characteristics 2、Corrected relevant content in package information
2025-1-13	V1.3	Added temperature range: -40 ~ +105℃

8 Contact information

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Post code: 102209

Feel free to contact us for any comment or suggestion during purchase and use.