ARM Cortex-M0+ 32-bit MCU, 64KB Flash, 16KB SRAM, 4xU(S)ART, 2xLPUART, I2C, 2xSPI, Timers, ADC, LCD, VREFBUF, AES, 1.8-5.5V

Datasheet

Features

- 48 MHz Cortex-M0+ 32-bit CPU
  Single-cycle multiplication instructions
- 64 KB Flash and 16 KB SRAM
- 1KB OTP
- Flexible power consumption management
  - Automatic switch of V_{BAT} backup power supply
  - 0.95 µA V_{BAT} mode+RTC+backup register
  - 1 µA Stop mode, CPU+SRAM retention
  - 1.25 µA Stop mode+RTC
  - 60µA/MHz@48MHz Run mode, in which peripherals are disabled
    Programs running in Flash
- Power detectors: BOR and PVD
- Clock sources
  - External high-speed clock: 4~32MHz, with CSS detection
  - External low-speed clock: 32.768 kHz, with CSS detection
  - Internal high-speed clock: 16MHz, full temperature variation within ±2%
  - Internal low-power, low-speed clock: 32 kHz
  - PLL: 6 MHz ~ 48MHz
- Up to 57 I/Os, anti-backflow, compatible with 5V communication, with the high drive I/O up to 20 mA
- 2-channel DMA controller to achieve flexible mapping
- RTC supporting alarm clock and periodic timer, with the calibration precision up to ±0.477ppm
- 9x timers
  - 3x 16-bit 4-channel general timers
  - 1x 16-bit basic timer
  - 2x 16-bit low-power timers, one of which supports -quadrature encoding
  - 1x 24-bit SysTick
  - 2x watchdogs: IWDG and WWDG
- IRTIM supporting timer and U(S)ART connection for infrared control
- Communication interfaces
  - 2x LPUART, supporting wakeup from Stop mode
  - 4x U(S)ART, one of which supports ISO7816 and SPI master modes; 3x UART
  - 2x SPI, with the maximum rate of 20 Mbps in master mode and 16 Mbps in slave mode
  - 1x I2C, master/slave mode, 1 Mbps Fm+, supporting wakeup from Stop mode
- Information security
  - AES algorithm coprocessor
  - TRNG, CRC
  - TAMP tamper-resistant and backup register
- LCD driver for up to 8 COM x 32 SEG
  - Charge pump mode: High drive capability, where V_{LCD} may rise to exceed V_{DD} without changing with V_{DD}; V_{LCD} is configurable in multiple levels up to 5.25 V
  - On-chip resistor voltage divider: Configurable 16 level contrasts, dynamically switch between high and low drive mode, without using external capacitors
- 12-bit 1 Msps high-accuracy SAR ADC can measure signals with high output impedance
- 2x ultra-low-power comparer with 6-bit DAC as the comparison reference, supporting rail-to-rail inputs
- Embedded reference voltage source VREFBUF at 3.0 V, 2.5 V, and 2.048 V, which can output through I/O
- 1x temperature sensor with the maximum tolerance of ±2 ℃
- 96-bit unique ID
- Embedded Bootloader: supporting UART
- Serial wire debug (SWD)
- Operating conditions: 1.8V~5.5V, -40 ℃~85 ℃
- Packages: LQFP64/48, QFN32, SSOP24

Declaration

The right to change the manual without notice to the user is reserved by CEC Huada Electronic Design Co., Ltd. Although we have reviewed the content of this manual, it is inevitable that it may still contain errors. As a result, we will periodically review the content of this manual and make necessary modification in the next release of the document. We recommend that you obtain the latest version from CEC Huada Electronic before finalizing your design.

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1 Introduction

The CIU32L051 ultra-low-power secure MCU is based on ARM Cortex-M0+ core. It is available in multiple packages, including LQFP64/48, QFN32 and SSOP24. The maximum frequency is up to 48 MHz. It supports independent backup power supply. Abundant peripherals are built in, including LCD, ADC, internal reference voltage source VREFBUF, ultra-low-power comparer, multiple LPUART/U(S)ART/I2C/SPI, RTC, multiple timers, and AES algorithm coprocessor.

Application scenarios of CIU32L051 ultra-low-power security MCUs:

- Portal medical devices
- Smart household appliances
- Smart fire protection
- Other low-power consumption scenarios powered by batteries

2 Product description

The CIU32L051 ultra-lower-power security MCU is equipped with 64 Kbytes of Flash and 16 Kbytes of SRAM, and other abundant peripherals. It is available in multiple packages, including LQFP64, LQFP48, QFN32 and SSOP24. The peripherals vary with the selected model and package form. For details, refer to the table below.

Table 2-1 CIU32L051 characteristics and peripherals

Peripheral		**CIU32L051**			
		R8T6	**C8T6**	**K8U6**	**E8M6**
Package		LQFP64	LQFP48	QFN32	SSOP24
Flash(Kbytes)		64			
SRAM(Kbytes)		16			
CPU		Cortex-M0+ core			
		Maximum frequency 48 MHz			
V_{BAT} mode		√			
Timer	General timer	3 (16-bit)			
	Basic timer	1 (16-bit)			
	LPTIM	2 (16-bit)			
	SysTick	1			
	IWDG	1			
	WWDG	1			
Communication interfaces	UART	3			
	USART	1 (supporting ISO7816 and SPI master mode)			
	LPUART	2			
	SPI	2			
	I2C	1 (supporting wakeup from Stop)			
RTC		√			
TAMP pin		1	1	×	×
AES		√			
CRC		√			
TRNG		√			
GPIOs		57	41	28	19

Peripheral	CIU32L051			
	R8T6	C8T6	K8U6	E8M6
LCD COM x SEG	4x36 6x34 8x32	4x22 6x20 8x18	×	×
12-bit ADC	15 external channels + 3 internal channels	14 external channels + 3 internal channels	7 external channels + 3 internal channels	7 external channels + 3 internal channels
VREFBUF	√			
Temp Sensor	√			
COMP	2			

3 Pin description

3.1 Pinouts

This chip is available in multiple packages, including LQFP64, LQFP48, QFN32, SSOP24, etc. The pinout is shown in the figure below.

Figure 3-1 CIU32L051R8T6-LQFP64 pinout

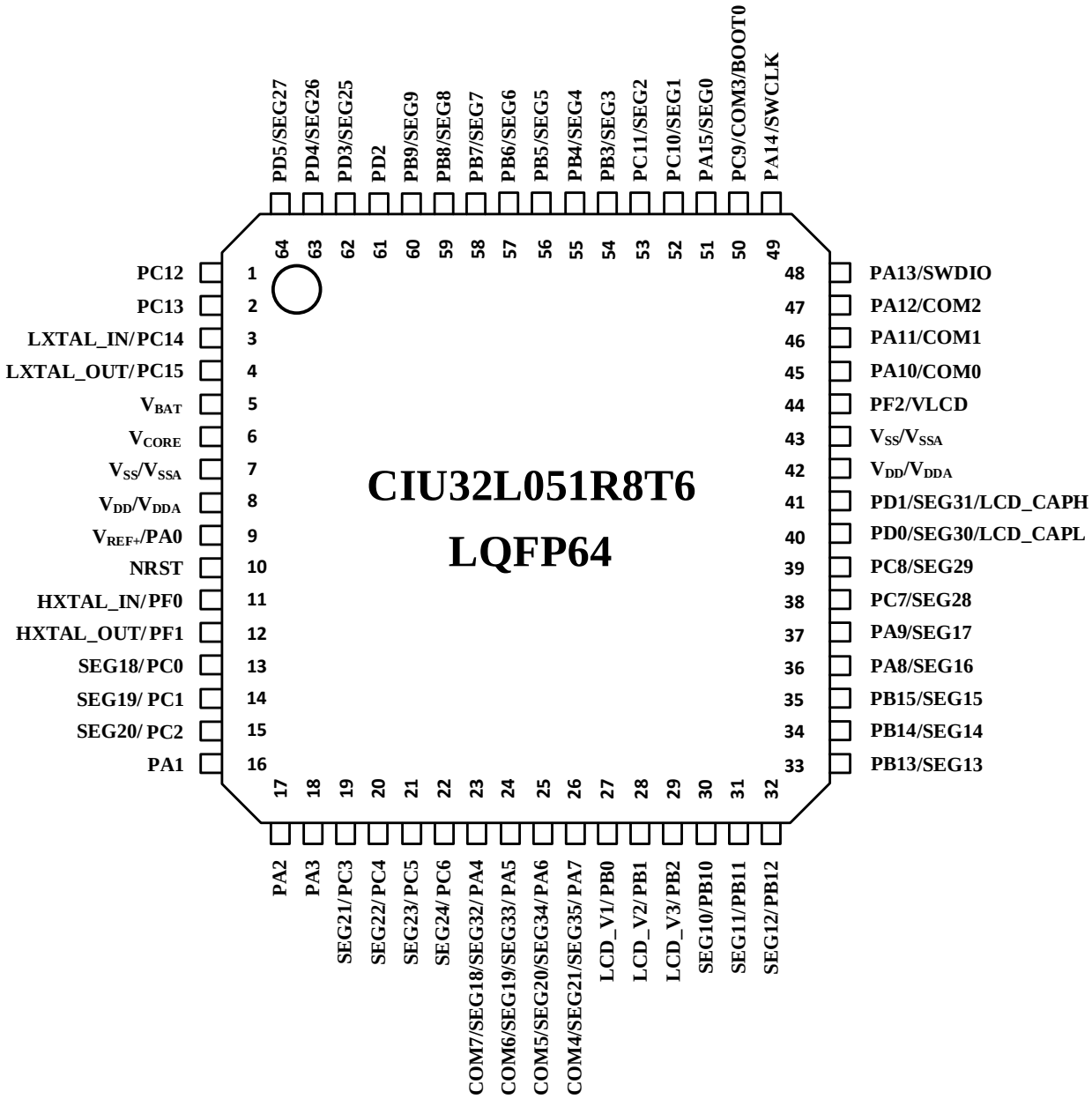


Figure 3-2 CIU32L051C8T6-LQFP48 pinout

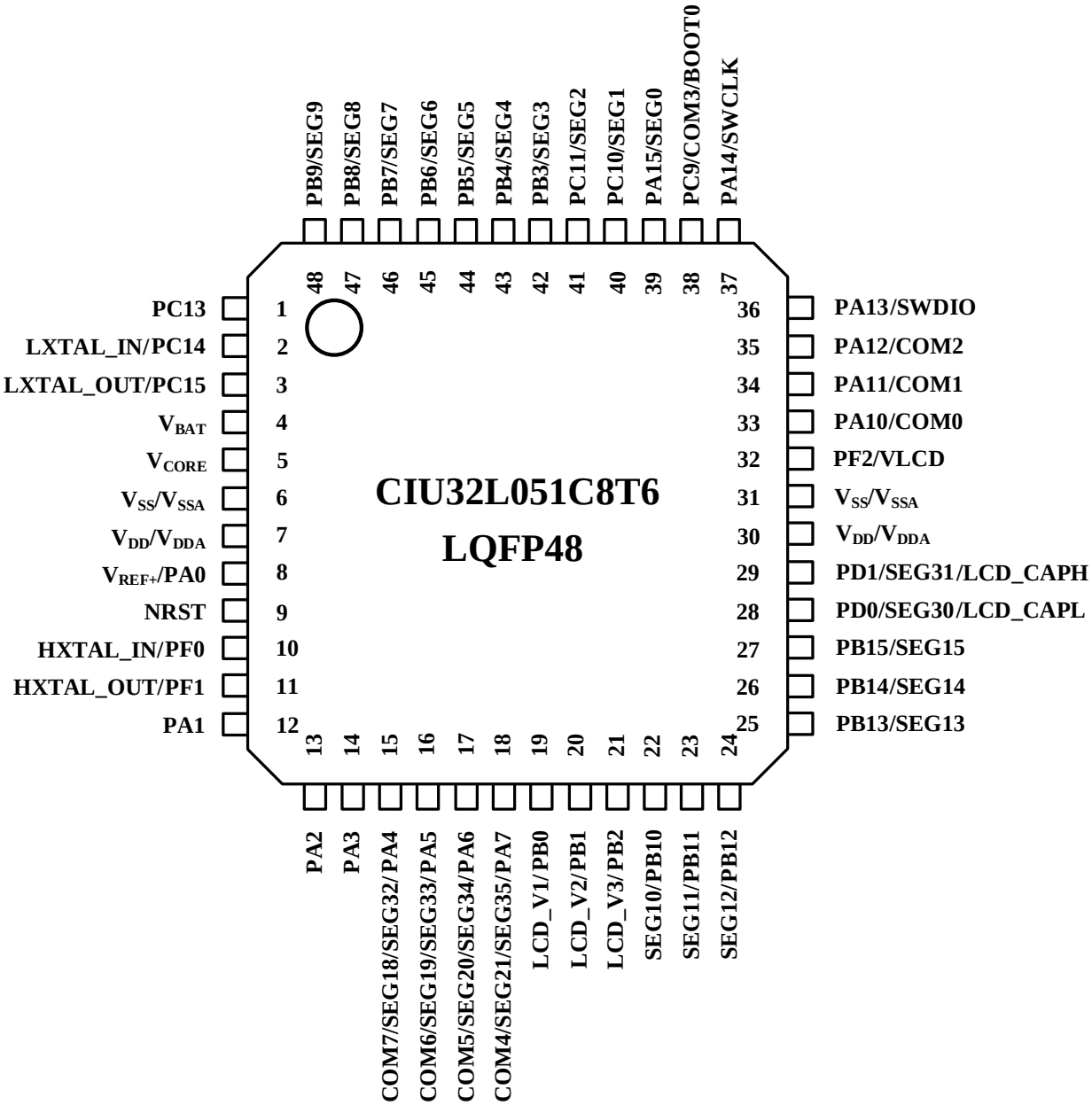
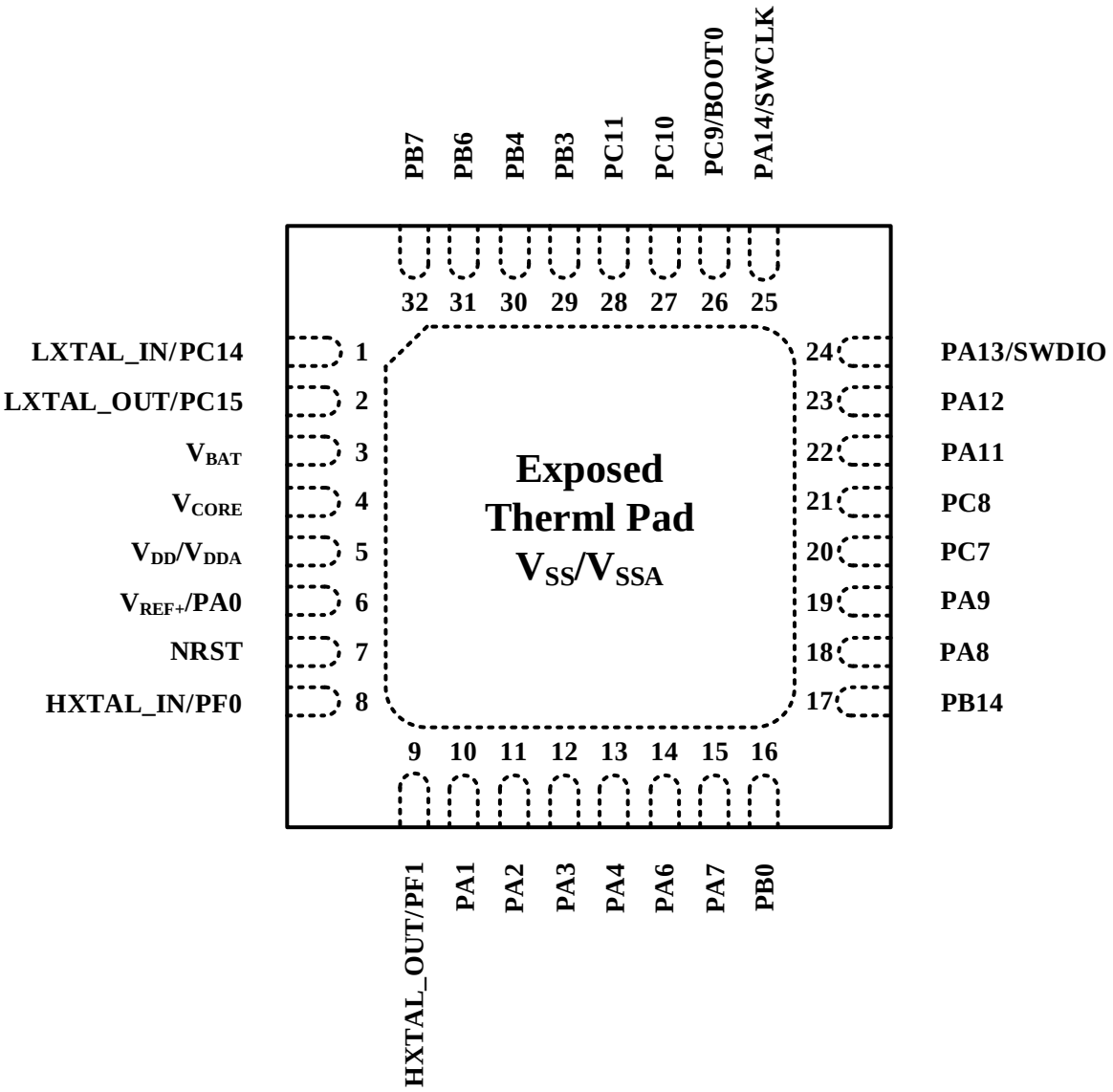
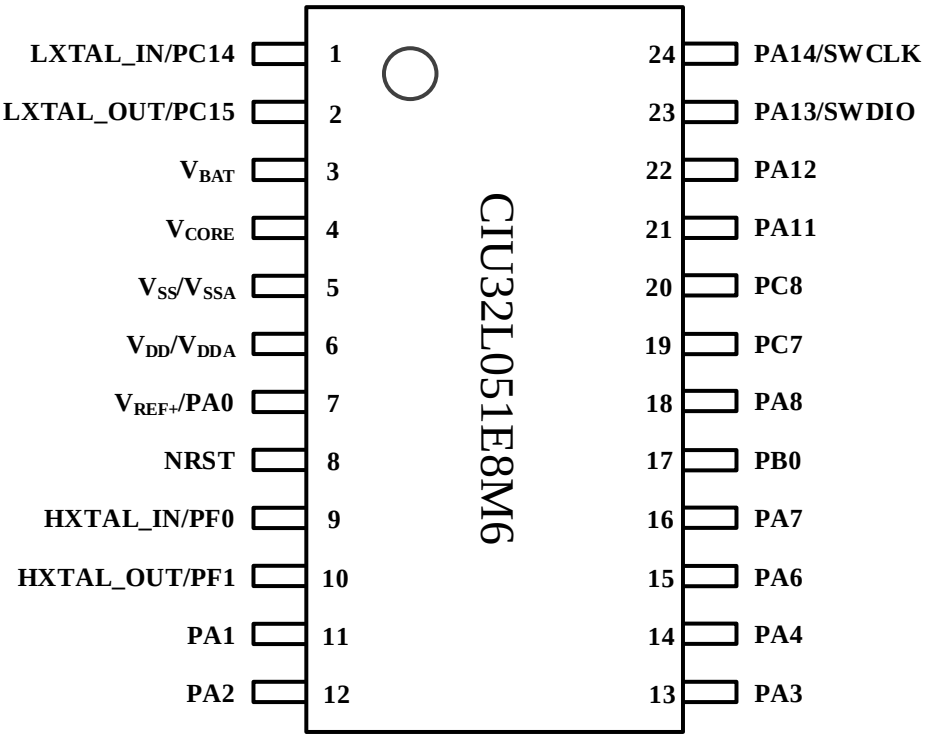


Figure 3-3 CIU32L051K8U6-QFN32 pinout



Note: For the QFN32 package, the Exposed Thermal Pad is V_{SS}/V_{SSA}, and must be connected to GND of the PCB.

Figure 3-4 CIU32L051E8M6-SSOP24 pinout



3.2 Pin definition

Table 3-1 Pin assignment and description

Pin No.				Pin name	Pin type	Drive capability	Additional functions	Alternate functions
LQFP64	LQFP48	QFN32	SSOP24					
1	-	-	-	PC12	I/O	Medium	ADC_IN19	UART3_TX TIM5_CH3 TIM4_CH2 IR_OUT
2	1	-	-	PC13	I/O	Low	TAMP_IN RTC_OUT	-
3	2	1	1	PC14	I/O	Low	LXTAL_IN	-
4	3	2	2	PC15	I/O	Low	LXTAL_OUT	-
5	4	3	3	V_{BAT}	P	-	-	-
6	5	4	4	V_{CORE}	P	-	-	-
7	6	-	5	V_{SS}/V_{SSA}	G	-	-	-
8	7	5	6	V_{DD}/V_{DDA}	P	-	-	-
9	8	6	7	V_{REF+}/PA0	I/O	Medium	-	SPI2_SCK USART1_CTS UART4_TX LPTIM1_OUT COMP1_OUT
10	9	7	8	NRST	I	Medium	NRST	-
11	10	8	9	PF0	I/O	Medium	HXTAL_IN	TIM5_CH3 UART2_TX UART4_RTS LPUART2_CTS LPUART1_CTS I2C1_SCL
12	11	9	10	PF1	I/O	Medium	HXTAL_OUT	TIM5_CH4 UART2_RX UART4_CTS LPUART2_RTS LPUART1_RTS I2C1_SDA
13	-	-	-	PC0	I/O	Medium	-	SPI2_SCK TIM4_CH1 LCD_SEG18

Pin No.				Pin name	Pin type	Drive capability	Additional functions	Alternate functions
LQFP64	LQFP48	QFN32	SSOP24					
								LPTIM1_OUT LPUART1_TX
14	-	-	-	PC1	I/O	Medium	-	SPI2_MISO TIM4_CH2 LCD_SEG19 LPTIM1_IN2 LPUART1_RX I2C1_SDA
15	-	-	-	PC2	I/O	Medium	-	SPI2_MOSI TIM4_CH3 LCD_SEG20 LPTIM1_IN1 I2C1_SCL
16	12	10	11	PA1	I/O	Medium	COMP2_INP ADC_IN0	SPI1_SCK USART1_RX TIM4_CH4 UART4_RX LPUART2_CTS
17	13	11	12	PA2	I/O	High Configurable	COMP2_INM ADC_IN1	SPI1_MOSI USART1_TX TIM4_CH1 MCO LPUART1_TX COMP2_OUT
18	14	12	13	PA3	I/O	Medium	ADC_IN2	SPI2_MISO USART1_RTS_DE _CK TIM4_CH2 UART4_TX MCO LPUART1_RX
19	-	-	-	PC3	I/O	Medium	COMP1_INM	USART1_TX LCD_SEG21 UART3_CTS LPTIM1_ETR
20	-	-	-	PC4	I/O	Medium	COMP1_INP	USART1_RX

Pin No.				Pin name	Pin type	Drive capability	Additional functions	Alternate functions
LQFP64	LQFP48	QFN32	SSOP24					
								LCD_SEG22 UART3_RTS UART3_RX
21	-	-	-	PC5	I/O	Medium	-	TIM3_CH1 USART1_RTS_DE_CK LCD_SEG23 UART3_TX LPUART1_TX
22	-	-	-	PC6	I/O	Medium	-	TIM3_CH2 USART1_CTS LCD_SEG24 UART3_RX LPUART1_RX
23	15	13	14	PA4	I/O	Medium	ADC_IN3 COMP1_INM	SPI1_NSS SPI2_MOSI TIM4_CH3 SEG32/SEG18/COM7 LPUART2_TX I2C1_SDA
24	16	-	-	PA5	I/O	Medium	ADC_IN4 COMP1_INP	SPI1_SCK IR_OUT TIM4_CH4 SEG33/SEG19/COM6 UART3_RTS LPUART2_RX I2C1_SCL COMP1_OUT
25	17	14	15	PA6	I/O	Medium	ADC_IN5	SPI1_MISO TIM3_CH1 SEG34/SEG20/COM5 UART3_CTS TIM5_CH1 LPUART1_CTS

Pin No.				Pin name	Pin type	Drive capability	Additional functions	Alternate functions
LQFP64	LQFP48	QFN32	SSOP24					
								LPTIM1_IN1
26	18	15	16	PA7	I/O	Medium	ADC_IN6	SPI1_MOSI TIM3_CH2 SEG35/SEG21/COM4 TIM4_CH1 LPTIM1_IN2 COMP2_OUT
27	19	16	17	PB0	I/O	Medium	ADC_IN7 LCD_V1	SPI1_NSS TIM3_CH3 UART3_RX LPTIM1_OUT COMP1_OUT
28	20	-	-	PB1	I/O	Medium	COMP1_INM ADC_IN8 LCD_V2	TIM3_CH4 UART3_RTS LPUART1_RTS
29	21	-	-	PB2	I/O	Medium	COMP1_INP ADC_IN9 LCD_V3	SPI2_MISO UART3_TX LPTIM1_OUT
30	22	-	-	PB10	I/O	Medium	ADC_IN10	SPI2_MOSI LCD_SEG10 UART3_TX LPUART1_RX COMP1_OUT
31	23	-	-	PB11	I/O	Medium	ADC_IN11	SPI2_SCK LCD_SEG11 UART3_RX LPUART1_TX COMP2_OUT
32	24	-	-	PB12	I/O	Medium	ADC_IN15	SPI2_NSS LCD_SEG12 LPUART1_RTS
33	25	-	-	PB13	I/O	Medium	ADC_IN16	SPI2_SCK TIM4_ETR LCD_SEG13 UART3_CTS

Pin No.				Pin name	Pin type	Drive capability	Additional functions	Alternate functions
LQFP64	LQFP48	QFN32	SSOP24					
								LPUART1_CTS
34	26	17	-	PB14	I/O	Medium	-	SPI2_MISO LCD_SEG14 UART3_RTS TIM4_CH1 LPUART2_CTS
35	27	-	-	PB15	I/O	Medium	-	SPI2_MOSI TIM4_CH2 LCD_SEG15 LPUART2_RTS COMP1_OUT
36	-	18	18	PA8	I/O	Medium	COMP1_INP	MCO SPI2_NSS UART3_TX LCD_SEG16 TIM4_CH3 LPTIM1_IN1 LPUART2_TX
37	-	19	-	PA9	I/O	Medium	COMP1_INM	MCO USART1_CTS UART3_RX LCD_SEG17 SPI2_MISO TIM4_CH4 LPUART2_RX LPTIM1_IN2
38	-	20	19	PC7	I/O	Medium	-	SPI1_NSS TIM3_CH3 TIM4_CH3 LCD_SEG28 LPUART2_RX UART3_RTS I2C1_SCL
39	-	21	20	PC8	I/O	Medium	-	SPI1_SCK TIM3_CH4 TIM4_CH4 LCD_SEG29

Pin No.				Pin name	Pin type	Drive capability	Additional functions	Alternate functions
LQFP64	LQFP48	QFN32	SSOP24					
								LPUART2_TX LPTIM1_OUT UART3_CTS I2C1_SDA
40	28	-	-	PD0	I/O	Medium	LCD_CAPL	SPI1_MOSI SPI2_NSS TIM5_CH1 LCD_SEG30 LPTIM1_IN1 UART3_RX
41	29	-	-	PD1	I/O	Medium	LCD_CAPH	SPI1_MISO SPI2_SCK TIM5_ETR LCD_SEG31 LPTIM1_IN2 UART3_TX
42	30	-	-	V_{DD}/V_{DDA}	P	-	-	-
43	31	-	-	V_{SS}/V_{SSA}	G	-	-	-
44	32	-	-	PF2	I/O	Medium	VLCD	SPI2_MISO USART1_CTS TIM4_ETR TIM5_CH1 LPTIM1_ETR
45	33	-	-	PA10	I/O	Medium	-	SPI2_MOSI USART1_RTS_DE_CK TIM4_CH4 LCD_COM0 TIM5_CH2 TIM5_CH1 TIM5_CH3
46	34	22	21	PA11	I/O	Medium	-	SPI1_MISO USART1_TX LCD_COM1 TIM5_CH3 TIM5_CH4

Pin No.				Pin name	Pin type	Drive capability	Additional functions	Alternate functions
LQFP64	LQFP48	QFN32	SSOP24					
								COMP1_OUT
47	35	23	22	PA12	I/O	Medium	-	SPI1_MOSI USART1_RX TIM4_ETR LCD_COM2 TIM5_CH4 COMP2_OUT
48	36	24	23	PA13	I/O	Medium	-	SWDIO USART1_TX IR_OUT LPUART2_TX
49	37	25	24	PA14	I/O	Medium	-	SWCLK USART1_RX LPUART2_RX
50	38	26	-	PC9	I/O	Medium	BOOT0	LCD_COM3
51	39	-	-	PA15	I/O	Medium	-	SPI1_NSS LCD_SEG0 UART4_RTS UART3_RTS
52	40	27	-	PC10	I/O	Medium	-	SPI2_MOSI UART3_RTS LCD_SEG1 TIM3_ETR
53	41	28	-	PC11	I/O	Medium	-	SPI2_MISO UART2_CTS LCD_SEG2 LPUART2_CTS
54	42	29	-	PB3	I/O	Medium	-	SPI1_SCK UART2_RTS TIM4_CH4 LCD_SEG3 LPUART2_RTS
55	43	30	-	PB4	I/O	Medium	-	SPI1_MISO UART2_CTS TIM3_CH1 LCD_SEG4

Pin No.				Pin name	Pin type	Drive capability	Additional functions	Alternate functions
LQFP64	LQFP48	QFN32	SSOP24					
								TIM5_ETR
56	44	-	-	PB5	I/O	Medium	-	SPI1_MOSI TIM3_CH2 LCD_SEG5 LPTIM1_IN1 COMP2_OUT
57	45	31	-	PB6	I/O	Medium	-	UART2_TX TIM5_CH3 LCD_SEG6 TIM5_CH2 LPTIM1_ETR
58	46	32	-	PB7	I/O	Medium	-	UART2_RX LCD_SEG7 UART4_CTS LPTIM1_IN2
59	47	-	-	PB8	I/O	Medium	-	MCO TIM4_ETR LCD_SEG8 TIM5_CH1 I2C1_SCL
60	48	-	-	PB9	I/O	Medium	-	IR_OUT LCD_SEG9 TIM5_CH2 I2C1_SDA
61	-	-	-	PD2	I/O	High Configurable	-	MCO USART1_RTS_DE_CK SPI1_NSS UART2_RTS LPTIM1_IN1 IR_OUT
62	-	-	-	PD3	I/O	Medium	-	SPI1_SCK USART1_TX LCD_SEG25 UART2_TX LPTIM1_IN2

Pin No.				Pin name	Pin type	Drive capability	Additional functions	Alternate functions
LQFP64	LQFP48	QFN32	SSOP24					
								TIM4_ETR TIM5_ETR
63	-	-	-	PD4	I/O	Medium	COMP2_INM	SPI1_MOSI UART4_TX TIM5_CH4 LCD_SEG26 UART2_RX LPTIM1_ETR USART1_RX TIM4_CH3
64	-	-	-	PD5	I/O	Medium	COMP2_INP	SPI1_MISO UART4_RX COMP2_OUT LCD_SEG27 UART2_RTS LPTIM1_OUT USART1_CTS TIM5_CH4

Table 3-2 I/O alternate function remapping

PORT	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI2_SCK	USART1_CTS	-	-	UART4_TX	LPTIM1_OUT	-	COMP1_OUT
PA1	SPI1_SCK	USART1_RX	TIM4_CH4	-	UART4_RX	-	LPUART2_CTS	-
PA2	SPI1_MOSI	USART1_TX	TIM4_CH1	-	-	MCO	LPUART1_TX	COMP2_OUT
PA3	SPI2_MISO	USART1_RTS_DE_CK	TIM4_CH2	-	UART4_TX	MCO	LPUART1_RX	-
PA4	SPI1_NSS	SPI2_MOSI	TIM4_CH3	SEG32/SEG18/COM7	-	LPUART2_TX	I2C1_SDA	-
PA5	SPI1_SCK	IR_OUT	TIM4_CH4	SEG33/SEG19/COM6	UART3_RTS	LPUART2_RX	I2C1_SCL	COMP1_OUT
PA6	SPI1_MISO	TIM3_CH1	-	SEG34/SEG20/COM5	UART3_CTS	TIM5_CH1	LPUART1_CTS	LPTIM1_IN1
PA7	SPI1_MOSI	TIM3_CH2	-	SEG35/SEG21/COM4	TIM4_CH1	-	LPTIM1_IN2	COMP2_OUT
PA8	MCO	SPI2_NSS	UART3_TX	LCD_SEG16	TIM4_CH3	LPTIM1_IN1	LPUART2_TX	-
PA9	MCO	USART1_CTS	UART3_RX	LCD_SEG17	SPI2_MISO	TIM4_CH4	LPUART2_RX	LPTIM1_IN2
PA10	SPI2_MOSI	USART1_RTS_DE_CK	TIM4_CH4	LCD_COM0	TIM5_CH2	TIM5_CH1	TIM5_CH3	-
PA11	SPI1_MISO	USART1_TX	-	LCD_COM1	TIM5_CH3	-	TIM5_CH4	COMP1_OUT
PA12	SPI1_MOSI	USART1_RX	TIM4_ETR	LCD_COM2	TIM5_CH4	-	-	COMP2_OUT
PA13	SWDIO	USART1_TX	IR_OUT	-	-	-	-	LPUART2_TX
PA14	SWCLK	USART1_RX	-	-	-	-	-	LPUART2_RX

PORT	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA15	SPI1_NSS	-	-	LCD_SEG0	UART4_RTS	UART3_RTS	-	-
PB0	SPI1_NSS	TIM3_CH3	-	-	UART3_RX	LPTIM1_OUT	-	COMP1_OUT
PB1	-	TIM3_CH4	-	-	UART3_RTS	-	LPUART1_RTS	-
PB2	SPI2_MISO	-	-	-	UART3_TX	LPTIM1_OUT	-	-
PB3	SPI1_SCK	UART2_RTS	TIM4_CH4	LCD_SEG3	-	-	LPUART2_RTS	-
PB4	SPI1_MISO	UART2_CTS	TIM3_CH1	LCD_SEG4	-	TIM5_ETR	-	-
PB5	SPI1_MOSI	-	TIM3_CH2	LCD_SEG5	-	LPTIM1_IN1	-	COMP2_OUT
PB6	-	UART2_TX	TIM5_CH3	LCD_SEG6	TIM5_CH2	LPTIM1_ETR	-	-
PB7	-	UART2_RX	-	LCD_SEG7	UART4_CTS	LPTIM1_IN2	-	-
PB8	MCO	-	TIM4_ETR	LCD_SEG8	-	TIM5_CH1	I2C1_SCL	-
PB9	-	IR_OUT	-	LCD_SEG9	-	TIM5_CH2	I2C1_SDA	-
PB10	SPI2_MOSI	-	-	LCD_SEG10	UART3_TX	-	LPUART1_RX	COMP1_OUT
PB11	SPI2_SCK	-	-	LCD_SEG11	UART3_RX	-	LPUART1_TX	COMP2_OUT
PB12	SPI2_NSS	-	-	LCD_SEG12	-	-	LPUART1_RTS	-
PB13	SPI2_SCK	TIM4_ETR	-	LCD_SEG13	UART3_CTS	-	LPUART1_CTS	-
PB14	SPI2_MISO	-	-	LCD_SEG14	UART3_RTS	TIM4_CH1	LPUART2_CTS	-
PB15	SPI2_MOSI	TIM4_CH2	-	LCD_SEG15	-	-	LPUART2_RTS	COMP1_OUT
PC0	-	SPI2_SCK	TIM4_CH1	LCD_SEG18	-	LPTIM1_OUT	LPUART1_TX	-
PC1	-	SPI2_MISO	TIM4_CH2	LCD_SEG19	-	LPTIM1_IN2	LPUART1_RX	I2C1_SDA
PC2	-	SPI2_MOSI	TIM4_CH3	LCD_SEG20	-	LPTIM1_IN1	-	I2C1_SCL
PC3	-	USART1_TX	-	LCD_SEG21	UART3_CTS	-	LPTIM1_ETR	-

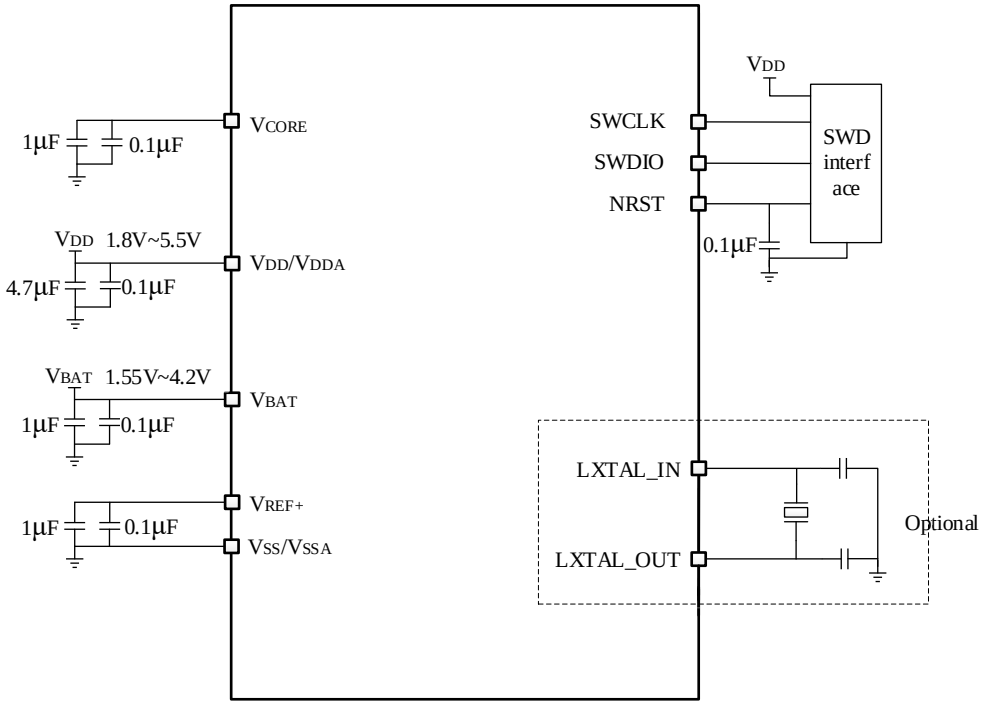
PORT	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC4	-	USART1_RX	-	LCD_SEG22	UART3_RTS	UART3_RX	-	-
PC5	-	TIM3_CH1	USART1_RTS_DE_CK	LCD_SEG23	UART3_TX	-	LPUART1_TX	-
PC6	-	TIM3_CH2	USART1_CTS	LCD_SEG24	UART3_RX	-	LPUART1_RX	-
PC7	SPI1_NSS	TIM3_CH3	TIM4_CH3	LCD_SEG28	LPUART2_RX	-	UART3_RTS	I2C1_SCL
PC8	SPI1_SCK	TIM3_CH4	TIM4_CH4	LCD_SEG29	LPUART2_TX	LPTIM1_OUT	UART3_CTS	I2C1_SDA
PC9	-	-	-	LCD_COM3	-	-	-	-
PC10	SPI2_MOSI	UART3_RTS	-	LCD_SEG1	TIM3_ETR	-	-	-
PC11	SPI2_MISO	UART2_CTS	-	LCD_SEG2	-	-	LPUART2_CTS	
PC12	-	UART3_TX	TIM5_CH3	-	TIM4_CH2	IR_OUT	-	-
PC13	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-
PD0	SPI1_MOSI	SPI2_NSS	TIM5_CH1	LCD_SEG30	-	LPTIM1_IN1	-	UART3_RX
PD1	SPI1_MISO	SPI2_SCK	TIM5_ETR	LCD_SEG31	-	LPTIM1_IN2	-	UART3_TX
PD2	MCO	USART1_RTS_DE_CK	SPI1_NSS	-	UART2_RTS	LPTIM1_IN1	-	IR_OUT
PD3	SPI1_SCK	USART1_TX	-	LCD_SEG25	UART2_TX	LPTIM1_IN2	TIM4_ETR	TIM5_ETR
PD4	SPI1_MOSI	UART4_TX	TIM5_CH4	LCD_SEG26	UART2_RX	LPTIM1_ETR	USART1_RX	TIM4_CH3
PD5	SPI1_MISO	UART4_RX	COMP2_OUT	LCD_SEG27	UART2_RTS	LPTIM1_OUT	USART1_CTS	TIM5_CH4
PF0	TIM5_CH3	UART2_TX	UART4_RTS	-	LPUART2_CTS	-	LPUART1_CTS	I2C1_SCL

PORT	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF1	TIM5_CH4	UART2_RX	UART4_CTS	-	LPUART2_RTS	-	LPUART1_RTS	I2C1_SDA
PF2	SPI2_MISO	USART1_CTS	TIM4_ETR	-	TIM5_CH1	LPTIM1_ETR	-	-

4 Circuitry of typical applications

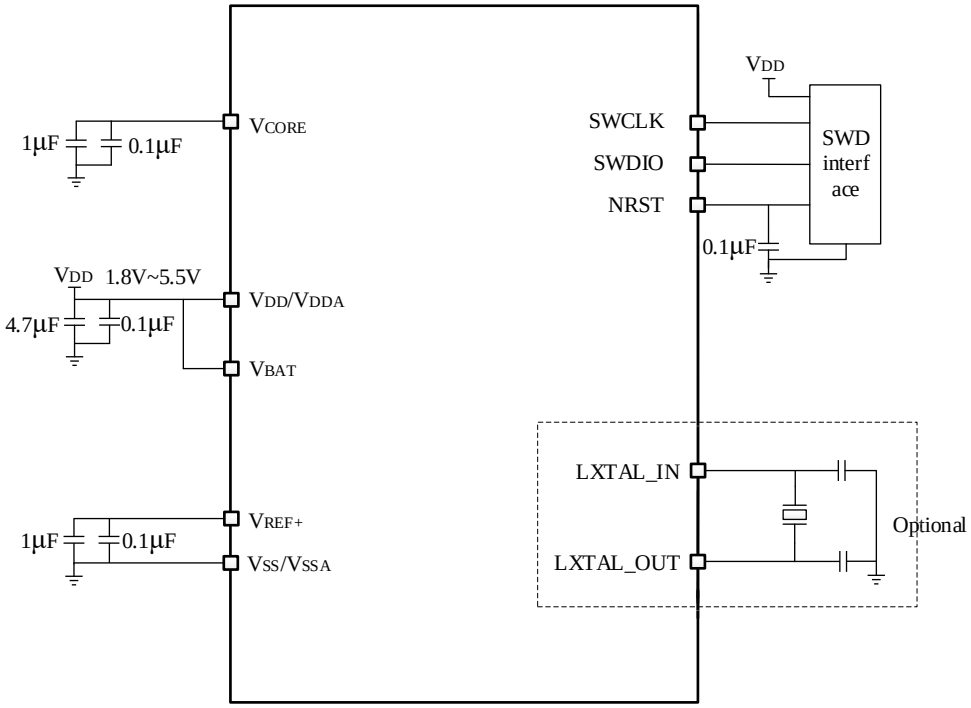
Note: Must select different EXTI channels when multiple I/O interrupts are used. Refer to the chapter of EXTI I/O selection register in the Reference Manual. For example, PA0, PB0, PC0… are on the same EXTI channel, and PA1, PB1, PC1… are on the same EXTI channel.

Typical application 1: V_{BAT} mode, automatic switch with the backup power supply



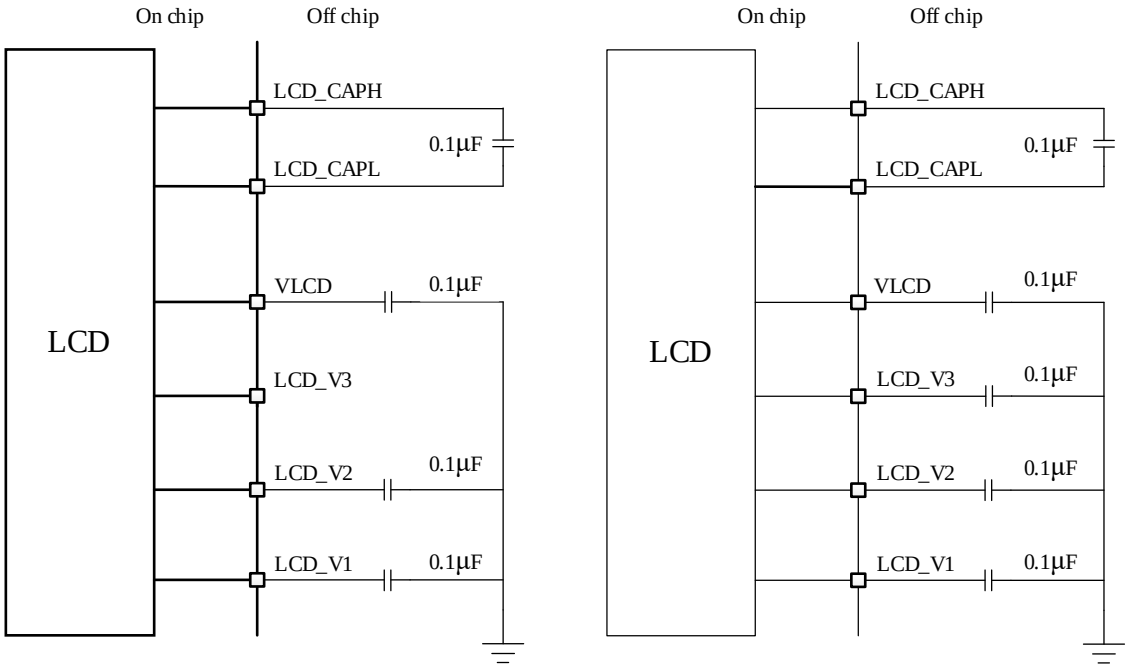
- The V_{DD} voltage range is 1.8V~5.5V;
- V_{BAT} is powered by the backup power supply or battery. The voltage range is 1.55V~4.2V. V_{BAT} pin should be connected to 1µF+0.1µF capacitor(the VBAT_MODE_EN bit in the flash option byte register FLASH_OPTR2 needs to be configured as 1 to enable the V_{BAT} mode);
- VREFBUF is enabled, and the V_{REF+} pin is connected to 1µF+0.1µF capacitor.

Typical application 2: Non-V_{BAT} mode, no backup power supply in use



- The V_{DD} voltage range is 1.8V~5.5V;
- V_{BAT} is connected to the V_{DD}/V_{DDA} pin, that is, not in the V_{BAT} mode(the VBAT_MODE_EN bit in the flash option byte register FLASH_OPTR2 needs to be configured as 0 to disable the V_{BAT} mode);
- VREFBUF is enabled, and the V_{REF+} pin is connected to 1μF+0.1μF capacitor.

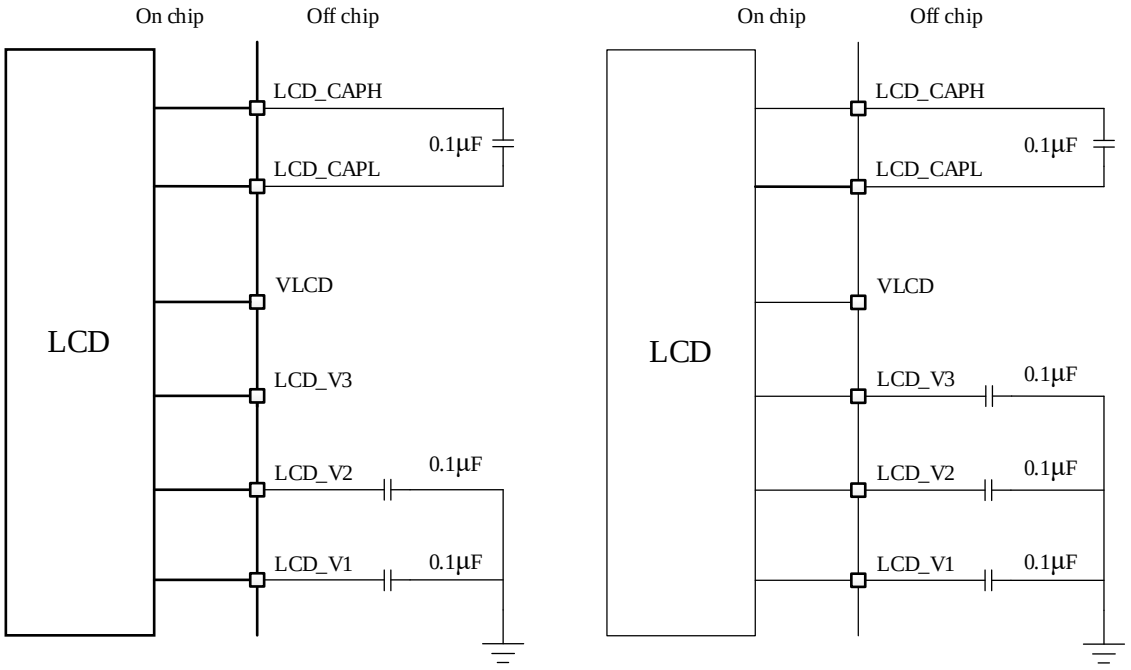
Typical application 3: LCD charge pump mode



1/3 bias　　1/4 bias

- LCD charge pump mode:
  - LCD_V3 is reused as GPIO at 1/3bias.

Typical application 4: Voltage division by LCD off-chip capacitor



1/3 bias　　1/4 bias

- Voltage division by LCD off-chip capacitor:
  - VLCD is reused as GPIO;
  - LCD_V3 is reused as GPIO at 1/3bias.

5 Electrical characteristics

5.1 Test conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

TBD indicates data to be defined.

5.2 Minimum and maximum values

Unless otherwise specified, the values are obtained through tests on 100% products in the production line at the temperature of T_A=25℃ and T_A=$T_A$max (where $T_A$max matches with the selected temperature range). All the minimum and maximum values can be guaranteed under the worst ambient temperature, power supply voltage, and clock conditions.

The data obtained through comprehensive assessment, designing simulation, and/or process characteristics as described in the notes below each table is not tested in the production line. On the basis of comprehensive assessment, the minimum and maximum values are normal distribution of average values multiplied or divided by three times after sample tests (mean ±3σ).

5.3 Typical values

Unless otherwise specified, typical values are based on T_A=25℃ and V_{DD}=3.3V ($1.8V \leq V_{DD} \leq 5.5V$).

5.4 Absolute maximum ratings

Stresses on the device above the values listed in the table below (voltage, current, and temperature) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External supply voltage	-0.3	6.5	V
V_{DDA}-V_{SS}	External analog supply voltage	-0.3	6.5	V
V_{BAT}-V_{SS}	V_{BAT} supply voltage	-0.3	6.5	V
V_{IN}	Pin input voltage(2)	V_{SS}-0.3	6.5	V

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power

supplies in the permitted range.

2. V_{IN} maximum values must always be followed. For the maximum allowed injected current values, refer to *Table: Current characteristics*.

Table 5-2 Current characteristics

Symbol	Description		Max	Unit
$I_{VDD/VDDA}$	Current into the V_{DD}/V_{DDA} power pin(1)		200	mA
$I_{VSS/VSSA}$	Current out of the V_{SS}/V_{SSA} ground pin(1)		200	
$I_{IO(PIN)}$ (2)	Output current sunk by I/O and control pins	PC13/PC14/PC15	3	
		PA2/PD2	20	
		Others	10	
	Output current sourced by I/O and control pins	PC13/PC14/PC15	3	
		PA2/PD2	20	
		Others	10	
$I_{INJ(PIN)}$(3)	I/O injected current		-5/0	
$\Sigma\|I_{INJ(PIN)}\|$(4)	Total injected current (sum of all I/O and control pins)		25	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies in the permitted range.
2. The output sink current and pull current of the I/O and control pins are the maximum currents at TA=25℃ and V_{DD}=3.3V and at V_{OL}=V_{SS}+0.5V and V_{OH}=V_{DD}-0.5V, respectively.
3. All I/Os have the anti-backflow functionality. No positive injected current is generated when $V_{IN} > V_{DD}$. When $V_{IN} < V_{SS}$, the negative injected current generated should be limited to be within 5 mA.
4. The maximum value of $\Sigma|I_{INJ(PIN)}|$ equals the sum of the absolute values of the positive injected current and the negative injected current (instantaneous values) when injected currents are present on multiple inputs at the same time.

Table 5-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	℃
T_J	Maximum junction temperature	105	℃

5.5 Operating conditions

5.5.1 General operating conditions

Table 5-4 General operating conditions

Symbol	Description	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	48	
f_{PCLK2}	Internal APB2 clock frequency	-	0	48	
V_{DD}	Digital supply voltage	-	1.8	5.5	V
V_{DDA}	Analog supply voltage	For ADC/COMP operation	1.8	5.5	
		For VREFBUF operation	2.4	5.5	
V_{BAT}	V_{BAT} supply voltage	The V_{BAT} pin is connected to the V_{DD}/V_{DDA} pin in the non-V_{BAT} mode.	1.8	5.5	V
		V_{BAT} is powered by the backup power supply in the V_{BAT} mode.	1.55	4.2	V
T_A	Ambient temperature	-	-40	85	℃
T_J	Junction temperature	-	-40	105	℃

5.5.2 Operating conditions at power-up/power-down

Table 5-5 Operating conditions at power-up/power-down

Symbol	Description	Condition	Min	Max	Unit
t_{VDD}	V_{DD} slew rate	V_{DD} rising	0	∞	μs/V
		V_{DD} falling: ULP_EN = 0	30	∞	
		V_{DD} falling: ULP_EN = 1	100	∞	ms/V

5.5.3 Embedded reset and power control block characteristics

Table 5-6 Embedded reset and power control block

Symbol	Description	Condition	Min(1)	Typ(2)	Max(1)	Unit
$t_{RSTTEMPO}$	POR temporization when V_{DD} crosses V_{POR}	V_{DD} rising	-	110	260	μs
V_{POR}	Power-on reset threshold	-	-	1.70	-	V
V_{PDR}	Power-down reset threshold	-	-	1.64	-	
V_{BOR0}	Brownout reset threshold 0	V_{DD} rising	1.96	2.11	2.18	
		V_{DD} falling	1.86	2.00	2.06	
V_{BOR1}	Brownout reset threshold 1	V_{DD} rising	2.14	2.30	2.37	
		V_{DD} falling	2.05	2.20	2.27	
V_{BOR2}	Brownout reset threshold 2	V_{DD} rising	2.43	2.61	2.69	
		V_{DD} falling	2.33	2.51	2.59	
V_{BOR3}	Brownout reset threshold 3	V_{DD} rising	2.71	2.91	3.00	
		V_{DD} falling	2.59	2.79	2.88	
V_{PVD0}	PVD threshold 0	Voltage rising	1.96	2.11	2.18	
		Voltage falling	1.86	2.00	2.06	
V_{PVD1}	PVD threshold 1	Voltage rising	2.14	2.30	2.37	
		Voltage falling	2.05	2.20	2.27	
V_{PVD2}	PVD threshold 2	Voltage rising	2.33	2.51	2.59	
		Voltage falling	2.22	2.39	2.47	
V_{PVD3}	PVD threshold 3	Voltage rising	2.43	2.61	2.69	
		Voltage falling	2.33	2.51	2.59	
V_{PVD4}	PVD threshold 4	Voltage rising	2.52	2.71	2.80	
		Voltage falling	2.43	2.61	2.69	
V_{PVD5}	PVD threshold 5	Voltage rising	2.71	2.91	3.00	
		Voltage falling	2.59	2.79	2.88	
V_{PVD6}	PVD threshold 6	Voltage rising	2.79	3.00	3.09	
		Voltage falling	2.71	2.91	3.00	
V_{PVD7}	PVD threshold 7	Voltage rising	2.87	3.09	3.19	
		Voltage falling	2.79	3.00	3.09	
$V_{hyst\_POR\_PDR}$	Hysteresis of V_{POR} and V_{PDR}		-	60	-	mV
$V_{hyst\_BOR\_PVD}$	Hysteresis of V_{BORx} and V_{PVDx}		-	100	-	mV

Symbol	Description	Condition	Min(1)	Typ(2)	Max(1)	Unit
$I_{DD(BOR)}$	BOR power consumption		-	0.4	0.6	μA
$I_{DD(PVD)}$	PVD power consumption		-	0.4	0.6	μA

1. Guaranteed by design. Not tested in production.
2. Derived from comprehensive assessment.

5.5.4 Embedded voltage reference

Table 5-7 Embedded voltage reference

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{BGR}	Embedded reference voltage	-40 ℃~85 ℃	1.181	1.200	1.213	V
t_{START}(1)	BGR startup time	-	-	10.3	30.2	μs
t_{SAMP} (1) (2)	Sampling time when reading the internal channel V_{BGR}	-	5	-	-	μs
t_{ADC_BUF}(1) (2)	Start time of the ADC internal channel V_{BGR} buffer	-	-	-	15	μs
$I_{DD(BGR)}$ (1)	BGR power consumption	V_{DD} = 3.3V	-	24.1	41.1	μA

1. Guaranteed by design. Not tested in production.
2. Wait for the startup stabilization time t_{ADC_BUF} to enable the ADC internal channel V_{BGR}. The sampling time for ADC to measure the internal channel V_{BGR} should be at least t_{SAMP}.

5.5.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is placed under the following conditions:

- All I/O pins are in the analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted with the minimum wait states number,

depending on the f_{HCLK} frequency (0 wait cycles for 0~16 MHz, 1 wait cycle for 16~32 MHz, and 2 wait cycles for over 32 MHz).

- When the peripherals are enabled: $f_{PCLK} = f_{HCLK}$.

Table 5-8 Current consumption in Run mode

Symbol	Description	Condition(1)				Typ	Unit
		Mode	Clock source	f_{HCLK}	Operating area		
$I_{DD(Run)}$	Supply current (Run mode)	All peripherals disabled; the CPU get instructions from Flash; Coremark	RCH clock source, PLL off	16MHz	Flash	1.65	mA
			RCH clock source, PLL on	32MHz		2.4	
				48MHz		2.95	
		All peripherals disabled; the CPU get instructions from Flash; While (1)	RCH clock source, PLL off	16MHz	Flash	0.95	
			RCH clock source, PLL on	32MHz		1.44	
				48MHz		1.8	
		All peripherals enabled; the CPU get instructions from Flash; While (1)	RCH clock source, PLL off	16MHz	Flash	1.73	
			RCH clock source, PLL on	32MHz		3.05	
				48MHz		4.15	

1. Test conditions: V_{DD} = 3.3V, T_A=25 ℃.

Table 5-9 Current consumption in Sleep mode

Symbol	Description	Condition(1)				Typ	Unit
		Mode	Clock source	f_{HCLK}	Operating area		
$I_{DD(Sleep)}$	Supply current (Sleep mode)	All peripherals disabled	RCH clock source, PLL off	16MHz	Flash	343	μA
			RCH clock source, PLL on	32MHz		594	
				48MHz		788	

1. Test conditions: V_{DD} = 3.3V, T_A=25 ℃。

Table 5-10 Current consumption in Stop mode

Symbol	Description	Condition		Typ				Unit
		Mode	V_{DD}	-40℃	25℃	55℃	85℃	
$I_{DD(Stop)}$	Supply current (Stop mode)	All peripherals disabled, Ultra-low power consumption enabled (ULP_EN=1)	1.8V	0.72	0.99	1.55	4.1	μA
			3.3V	0.76	1.02	1.6	4.35	
			5.5V	0.84	1.1	1.78	4.97	
		RTC enabled: clocked by LXTAL, LXTAL_DRV_MODE=0, LXTAL_DRV[1:0]=00, Other peripherals disabled, Ultra-low power consumption enabled (ULP_EN=1)	1.8V	0.93	1.2	1.8	4.24	
			3.3V	1	1.25	1.92	4.53	
			5.5V	1.19	1.48	2.28	5.3	

Table 5-11 Current consumption in V_{BAT} mode

Symbol	Description	Condition(1)		Typ	Unit
		Mode	V_{BAT}		
$I_{DD(VBAT)}$	Supply current (V_{BAT} mode)	V_{BAT} mode: RTC enabled, clocked by LXTAL, LXTAL_DRV_MODE=0, LXTAL_DRV[1:0]=00	1.8V	0.92	μA
			3.3V	0.95	
			4.2V	0.98	
		Storage mode: Only V_{BAT} is powered on and V_{DD} has never been powered on	3.3V	10	nA

1. Test conditions: T_A=25℃.

5.5.6 Wakeup time from low-power modes

The wakeup times are the latency between the event and the execution of the first user instruction.

Table 5-12 Wakeup time from low-power modes(1)

Symbol	Description	Condition	Typ	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode	Transiting to Run-mode execution in Flash memory: HCLK = RCH = 16MHz	12	CPU cycles
t_{WUSTOP}	Wakeup time from Stop mode	Transiting to Run-mode execution in Flash memory: HCLK = RCH = 16MHz	17.3	μs

1. Derived from comprehensive assessment.

5.5.7 External clock source characteristics

HXTAL bypass mode

Table 5-13 HXTAL oscillator characteristic in bypass mode (1)

Symbol	Description	Min	Typ	Max	Unit
f_{HXTAL}	High-speed external clock (HXTAL) frequency	-	-	48	MHz
V_{HXTALH}	HXTAL_IN input pin high level voltage	1.05	-	V_{DD}	V
V_{HXTALL}	HXTAL_IN input pin low level voltage	V_{SS}	-	0.45	

1. Derived from comprehensive assessment.

HXTAL external crystal mode

The high-speed external clock (HXTAL) can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is obtained from comprehensive characteristic assessment with typical external components specified in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins in order to minimize the output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.).

Table 5-14 HXTAL oscillator characteristic in external crystal mode (1)

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{HXTAL}	Oscillator frequency	-	4	-	32	MHz
I_{DD_HXTAL}(2)	HXTAL current consumption	Low drive	-	0.28	-	mA
		Medium low drive	-	0.68	-	
		Medium high drive	-	1.18	-	
		High drive	-	1.55	-	
R_F	Feedback resistor	-	-	600	-	kΩ
G_{mcrit}(3)	Maximum critical crystal transconductance	Low drive	-	-	0.55	mA/V
		Medium low drive	-	-	1.53	

Symbol	Description	Condition	Min	Typ	Max	Unit
		Medium high drive	-	-	3.07	
		High drive	-	-	3.43	
$t_{SU}+t_{STAB}$(4)	Startup stabilization time	High drive CL = 10pF @8MHz	-	600	-	μs

1. Guaranteed by design. Not tested in production.
2. Test crystal conditions: V_{DD} = 3.3V, CL = 10pF@8MHz.
3. Maximum oscillation start transconductance of the external crystal resonator supported by the chip.
4. $t_{SU}+t_{STAB}$ is the startup time measured from the moment it is enabled (by software) to a stabilized oscillation is reached. This value is measured for an 8 MHz standard crystal resonator. It can vary significantly with the crystal manufacturer.

LXTAL external crystal mode

The low-speed external clock (LXTAL) can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is obtained from comprehensive characteristic assessmentwith typical external components specified in the table below. In the application, the resonator and the load capacitors must be as close as possible to the oscillator pins in order to minimize the output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.).

Table 5-15 LXTAL oscillator characteristics in external crystal mode (1)

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{LXTAL}	Oscillator frequency	-	-	32.768	-	KHz
I_{DD_LXTAL}	LXTAL current consumption in common mode	Low drive	-	170	-	nA
		Medium low drive	-	200	-	
		Medium high drive	-	230	-	
		High drive	-	260	-	
	LXTAL current consumption in enhanced mode	Low drive	-	240	-	
		Medium low drive	-	275	-	

Symbol	Description	Condition	Min	Typ	Max	Unit
		Medium high drive	-	315	-	
		High drive	-	370	-	
R_F	Feedback resistance	-	-	10.8	-	MΩ
G_{mcrit}(2)	Maximum critical crystal transconductance	Low drive	-	-	1.18	μA/V
		Medium low drive	-	-	3.04	
		Medium high drive	-	-	4.73	
		High drive	-	-	7.60	
$t_{SU}+t_{STAB}$(3)	Startup stabilization time	High drive CL = 12.5pF @32.768KHz	-	300	-	ms

1. Guaranteed by design. Not tested in production.
2. Maximum oscillation start transconductance of the external crystal resonator supported by the chip.
3. t_{SU} +t_{STAB} is the startup time measured from the moment it is enabled (by software) to a stabilized oscillation is reached. This value is measured for an 32.768 kHz standard crystal resonator. It can vary significantly with the crystal manufacturer and model.

5.5.8 Internal clock source characteristics

RCH（16MHz）

Table 5-16 Internal RCH oscillator characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{RCH}	RCH frequency	-	-	16	-	MHz
I_{DD_RCH}(1)	RCH oscillator power consumption	-	-	96	106	μA
$\Delta Temp_{(RCH)}$	RCH frequency drift over temperature	V_{DD}=1.8V~5.5V T_A= -40℃ ~ 85℃	-2	-	2	%
$Duty_{(RCH)}$ (2)	RCH Duty cycle	-	45	-	55	%
$t_{SU(RCH)}$ (2)	RCH startup time	-	-	0.97	-	μs
$t_{STAB(RCH)}$ (2)	RCH stabilization time	-	-	0.31	-	μs

1. Derived from comprehensive assessment.
2. Guaranteed by design. Not tested in production.

RCL（32KHz）

Table 5-17 Internal RCL oscillator characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{RCL}	RCL frequency	V_{DD}=1.8V~5.5V T_A= -40 ℃~85 ℃	28.2	32	35.1	KHz
I_{DD_RCL}(1)	RCL oscillator power consumption	-	-	135	-	nA
Duty(2)	Duty cycle	-	47	-	53	%
$t_{SU(RCL)} + t_{STAB(RCL)}$ (2)	RCL startup stabilization time	-	-	134	-	μs

1. Derived from comprehensive assessment.
2. Guaranteed by design. Not tested in production.

5.5.9 PLL characteristics

Table 5-18 PLL characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock frequency	-	4	-	32	MHz
$Duty_{(PLL\_IN)}$	PLL input clock duty cycle	-	45	-	55	%
f_{PLL_OUT}	PLL output clock frequency	-	6	-	48	MHz
$Duty_{(PLL\_OUT)}$	PLL output clock duty cycle	-	45	-	55	%
t_{LOCK}	PLL lock time	-	-	34	50	μs

1. Guaranteed by design. Not tested in production.

5.5.10 Flash memory characteristics

Table 5-19 Flash memory characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
t_{PROG}	Word programming time	-	-	50	-	μs
	Fast programming (64 words)	-	-	1.97	-	ms
t_{ERASE}	Erase time	Page erase	-	2.5	-	ms

Symbol	Description	Condition	Min	Typ	Max	Unit
		Mass erase	-	35	-	ms
EC_{Flash}	Endurance	T_A= 25 ℃	20000	-	-	Cycles
		T_A= -40 ℃~85 ℃	10000	-	-	
RET_{Flash}	Data retention	T_A= 85 ℃	25	-	-	Years

1. Derived from comprehensive assessment.

5.5.11 EFT characteristics

Table 5-20 EFT characteristics(1)

Symbol	Description	Condition	Level/type
V_{EFTB}	Fast transient voltage burst limits to be applied on V_{DD} and V_{SS} pin to induce a functional disturbance	T_A = 25 ℃ According to IEC 61000-4-4	5A

1. Derived from comprehensive assessment.

5.5.12 ESD characteristics

Table 5-21 ESD characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Human body model	T_A = 25 ℃ According to ESDA/JEDEC JS-001-2017	-	±6000	-	V
$V_{ESD(CDM)}$	Charge device model	T_A = 25 ℃ According to ESDA/JEDEC JS-002-2018	-	±2000	-	
$V_{ESD(MM)}$	Mechanical model	T_A = 25 ℃ According to JESD22-A115C	-	±300	-	

1. Derived from comprehensive assessment.

Table 5-22 Latch-up characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
$I_{Latch-up}$	Latch-up current	T_A = 25 ℃ According to JEDEC78E	-	±400	-	mA

1. Derived from comprehensive assessment.

5.5.13 I/O port characteristics

Table 5-23 Input characteristics

Symbol	Description	Condition		Min	Typ	Max	Unit
V_{IL}(1)	Input low level voltage	PC13/PC14/PC15	1.8V≤V_{DD}≤5.5V	-	-	0.3V_{DD}	V
		PA2/PD2		-	-	0.3V_{DD}	
		Others		-	-	0.3V_{DD}	
V_{IH}(1)	Input high level voltage	PC13/PC14/PC15	1.8V≤V_{DD}≤5.5V	0.7V_{DD}	-	-	
		PA2/PD2		0.7V_{DD}	-	-	
		Others		0.7V_{DD}	-	-	
V_{hys}(1)	Schmitt trigger voltage hysteresis	PC13/PC14/PC15	V_{DD}=3.3V	-	200	-	mV
		PA2/PD2		-		-	
		Others		-		-	
I_{lkg}(1)	Input leakage current	PC13/PC14/PC15	V_{DD}=3.3V	-	2	-	nA
		PA2/PD2		-		-	
		Others		-		-	
R_{PU}(2)	Weak pull-up equivalent resistor	V_{IN} = V_{SS}		20	37	60	kΩ
R_{PD}(2)	Weak pull-down equivalent resistor	V_{IN} = V_{DD}		20	37	60	kΩ
C_{IO}(2)	I/O pin capacitance	PC13/PC14/PC15		-	1.22	-	pF
		PA2/PD2		-	1.85	-	
		Others		-	1.30	-	

1. Derived from comprehensive assessment.
2. Guaranteed by design. Not tested in production.

Table 5-24 Output characteristics(1)

Symbol	Description	Condition		Min	Typ	Max	Unit
V_{OL}(1)	Output low level voltage	PC13/PC14/PC15	$\|I_{IO}\|$ = 1.5mA V_{DD} = 3.3V	-	0.18	-	V
		PA2/PD2	$\|I_{IO}\|$ = 10mA V_{DD} = 3.3V	-	0.26	-	
		Others	$\|I_{IO}\|$= 5mA V_{DD} = 3.3V	-	0.25	-	

Symbol	Description	Condition		Min	Typ	Max	Unit
V_{OH}(2)	Output high level voltage	PC13/PC14/PC15	$\|I_{IO}\|$ = 1.5mA V_{DD} = 3.3V	-	3.08	-	
		PA2/PD2	$\|I_{IO}\|$=10mA V_{DD} = 3.3V	-	3.04	-	
		Others	$\|I_{IO}\|$=5mA V_{DD} = 3.3V	-	3.05	-	

1. Derived from comprehensive assessment.
2. The I_{IO} sink current must follow the absolute maximum ratings listed in *Table: Current characteristics*, and the total current of I_{IO} (I/O port and control pin) shall not exceed $I_{VSS/VSSA}$.
3. The I_{IO} pull current must follow the absolute maximum ratings listed in *Table: Current characteristics*, and the total current of I_{IO} (I/O port and control pin) shall not exceed $I_{VDD/VDDA}$.

Table 5-25 AC characteristics(1)

Symbol	Description	Condition	Min	Max	Unit
f_{MAX}	Maximum output frequency	C=50pF , 1.8V≤V_{DD}＜2.7V	-	10	MHz
		C=50pF, 2.7V≤V_{DD}≤5.5V	-	20	
		C=30pF , 1.8V≤V_{DD}＜2.7V		16	
		C=30pF , 2.7V≤V_{DD}≤5.5V	-	32	
T_r	Rise time	C=50pF , 1.8V≤V_{DD}＜2.7V	-	24.71	ns
		C=50pF , 2.7V≤V_{DD}≤5.5V	-	14.81	
		C=30pF , 1.8V≤V_{DD}＜2.7V	-	16.72	
		C=30pF , 2.7V≤V_{DD}≤5.5V	-	10.07	
T_f	Fall time	C=50pF , 1.8V≤V_{DD}＜2.7V	-	27.82	ns
		C=50pF , 2.7V≤V_{DD}≤5.5V	-	17.15	
		C=30pF , 1.8V≤V_{DD}＜2.7V	-	18.37	
		C=30pF , 2.7V≤V_{DD}≤5.5V	-	11.25	

1. Guaranteed by design. Not tested in production.

5.5.14 NRST input characteristics

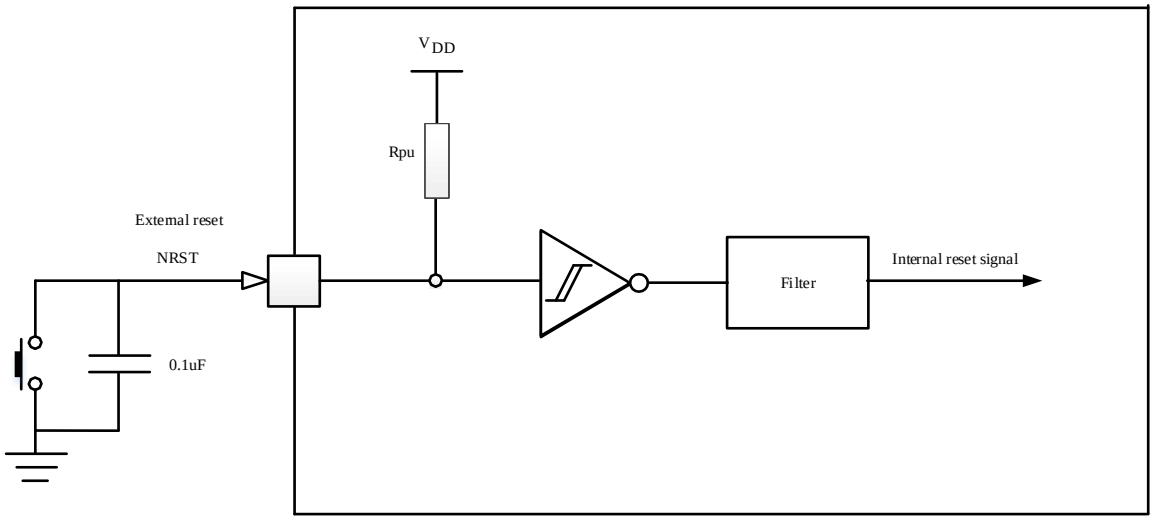
The NRST pin is connected to a permanent internal pull-up resistor. Therefore, it is not necessary to connect to an external pull-up resistor.

Table 5-26 NRST input characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
$V_{IL\ (NRST)}$	Input low-level voltage	-	-	-	$0.3V_{DD}$	V
$V_{IH\ (NRST)}$	Input high-level voltage	-	$0.7V_{DD}$	-	-	
$V_{hys\ (NRST)}$	Schmitt trigger voltage hysteresis	-	-	300	-	mV
R_{PU}	Pull-up equivalent resistor	$V_{IN}=V_{SS}$	6	10	18	kΩ
$T_{(NRST)}$ (2)	Filtered pulse	$1.8V \leqslant V_{DD} \leqslant 5.5V$	500			μs

1. Guaranteed by design. Not tested in production.
2. The low-level signal on the NRST pin must be greater than 500 μs to reset the chip.

Figure 5-1 Recommended circuit for the NRST pin



1. The reset circuit can protect the MCU to avoid resets caused by noise interference.
2. The user must ensure that the electrical level on the NRST pin can be reduced to below the V_{IL} maximum level listed in the table of I/O input characteristics; otherwise, no reset is executed.
3. The external capacitor on NRST pin must be placed as close as possible to the device.

5.5.15 ADC characteristics

Table 5-27 ADC characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	5.5	V
V_{REF_ADC}	Reference voltage	-	1.8	-	V_{DDA}	V
f_{ADC_CK}	ADC clock frequency	$2.4V < V_{DDA} \leq 5.5V$	0.6	-	16	MHz

Symbol	Description	Condition	Min	Typ	Max	Unit
		1.8V≤V_{DDA}≤2.4V	0.6	-	8	
f_S	Sampling rate	12 bits	-	-	1	Msps
V_{AIN}	Conversion voltage range	-	V_{SSA}	-	V_{REF+}	V
R_S	Input switch equivalent impedance	-	-	0.44	15	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	8	-	pF
t_{STAB}	ADC power-up time	f_{ADC_CK}≥6MHz	-	-	2.5	μs
		f_{ADC_CK}＜6MHz	-	-	17	$1/f_{ADC\_CK}$
t_{CAL}	Calibration time	-	-	112	-	$1/f_{ADC\_CK}$
t_{LATR}	Trigger conversion latency	CKSRC = 00	-	4.5	-	$1/f_{ADC\_CK}$
		CKSRC = 01	-	4.25	-	
		CKSRC = 10	-	4.125	-	
t_{SAMP}	Sampling time	-	3	-	1919	$1/f_{ADC\_CK}$
t_{CONV}	Total conversion time (including sampling time)	-	t_{SAMP} + 13			$1/f_{ADC\_CK}$
$I_{DDA(ADC)}$	ADC consumption from V_{DDA}	fs = 1Msps	-	390	-	μA
$I_{DDV(ADC)}$	ADC consumption from V_{REF+}	fs = 1Msps	-	40	-	μA
t_{IDLE}	Laps of time allowed between two conversions	-	-	-	440	μs

1. Guaranteed by design. Not tested in production.

Table 5-28 Sampling time and input signal impedance(1) (2)

Resolution	Sampling cycle (16 MHz)	Sampling time (16 MHz) (μs)	Maximum input impedance R_{AIN} (kΩ)
12bits	3	0.188	2.6
	7	0.438	3.1
	12	0.75	3.6
	19	1.188	8.8
	39	2.438	14.2
	79	4.938	30
	119	7.438	50

Resolution	Sampling cycle (16 MHz)	Sampling time (16 MHz) (μs)	Maximum input impedance R_{AIN} (kΩ)
	159	9.938	67
	239	14.938	84
	319	19.938	124
	479	29.938	182
	639	39.938	223
	959	59.938	320
	1279	79.938	645
	1919	119.938	850

1. Derived from comprehensive assessment.
2. The value in the table is the input impedance when the sample tolerance is smaller than 10 LSB.

Table 5-29 ADC accuracy(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
EO	Offset error	$V_{DDA} = V_{REF\_ADC}$ = 3.3 V; fs= 1 Msps; T_A = 25 ℃	-	-3	-	LSB
EG	Gain error		-	6	-	LSB
DNL	Differential nonlinear error		-	2	-	LSB
INL	Integral nonlinear error		-	3	-	LSB
SNR	Signal-to-noise ratio	$V_{DDA} = V_{REF\_ADC}$ = 3.3 V; fs= 1 Msps; T_A = 25 ℃; f_{IN}=1KHz	-	63	-	dB
SINAD	Signal-to-noise and distortion ratio		-	62	-	dB
THD	Total harmonic distortion		-	-70	-	dB
ENOB	Effective number of bits		-	10	-	bit

1. Derived from comprehensive assessment.

5.5.16 VREFBUF characteristics

Table 5-30 VREFBUF characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit

Symbol	Description	Condition		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	VRS = 00		2.4	-	5.5	V
		VRS = 01		2.8	-	5.5	
		VRS = 10		3.3	-	5.5	
V_{OUT}(2)	Output voltage	VRS = 00	2.4V≤VDDA≤5V	2.043	2.048	2.053	V
		VRS = 01	2.8V≤VDDA≤5V	2.495	2.5	2.505	
		VRS = 10	3.3V≤VDDA≤5V	2.99	3.0	3.01	
V_{trim}	Trim step resolution	-		-	±0.1	-	%
C_L	Load capacitor	-		0.5	1.1	1.5	μF
t_{STAB}	Startup stabilization time	VRS = 00	C_L=1.1μF	-	340	640(3)	μs
		VRS = 01		-	400	760(3)	
		VRS = 10		-	460	900(3)	
I_{LOAD}	Static load current	-		-	-	2	mA
I_{DD}	Power consumption from I_{DD}	I_{LOAD}=0μA~2mA		-	13.7	18.9(3)	μA

1. Derived from comprehensive assessment.
2. The typical, maximum, and minimum values are guaranteed at T_A = 25 ℃ in production test.
3. Guaranteed by design. Not tested in production.

5.5.17 COMP characteristics

Table 5-31 COMP characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
$V_{DDA(COMP)}$	Analog supply voltage	-	1.8	-	5.5	V
V_{IN}	COMP Input voltage	-	0	-	V_{DDA}	V
t_{START}	Startup time	High-speed	-	4.0	-	μs
		Medium-speed	-	4.5	-	
		Low-speed	-	7.0	-	
		Ultra-low-speed	-	8.4	-	
V_{offset}(2)	Offset voltage	-	-10.8	-	8.4	mV
V_{hys}	Hysteresis	No hysteresis	-	0	-	mV
		Low hysteresis	-	10	-	
		Medium hysteresis	-	20	-	

Symbol	Description	Condition	Min	Typ	Max	Unit
		High hysteresis	-	30	-	
t_D	Propagation delay	High-speed	-	0.08	-	μs
		Medium-speed	-	0.15	-	
		Low-speed	-	0.98	-	
		Ultra-low-speed	-	3.46	-	
I_{COMP}	Static power consumption	High-speed	-	22.63	-	μA
		Medium-speed	-	12.34	-	
		Low-speed	-	1.59	-	
		Ultra-low-speed	-	0.53	-	

1. Derived from comprehensive assessment.
2. Guaranteed by design. Not tested in production.

5.5.18 Temperature sensor characteristics

Table 5-32 Temperature sensor characteristics(1)

Symbol	Description	Min	Typ	Max	Unit
T_L	V_{TS} linearity with temperature	-	±1	±2	℃
Avg_Slope	Average slope	-	3.02	-	mV/℃
V_{25}	Voltage at 25℃ (±5℃)	-	898	-	mV
$I_{DDA(TS)}$	Temperature sensor consumption from V_{DDA}	-	14.5	-	μA
t_{ADC_BUF}(2)	Startup time of the temperature sensor V_{TS} Buffer	-	-	17.3	μs
t_{SAMP} (2)	ADC sampling time when reading the temperature	5	-	-	μs

1. Guaranteed by design. Not tested in production.
2. Wait for the startup stabilization time t_{ADC_BUF} to enable the ADC internal temperature sensor. The sampling time for ADC to measure the temperature sensor should be at least t_{SAMP}.

5.5.19 V_{BAT} and V_{DDA} monitoring characteristics

Table 5-33 V_{BAT} and V_{DDA} monitoring characteristics(1)

Symbol	Description	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT} and V_{DDA}	-	34	-	kΩ

Symbol	Description	Min	Typ	Max	Unit
	input channels inside ADC				
Q	Ratio on voltage measurement	-	3	-	-
Er	Error on Q	-1	0.26	1	%
t_{ADC_BUF}(2)	Startup time of the V_{BAT} and V_{DDA} input channel Buffer	-	-	15	μs
t_{SAMP}(2)	ADC sampling time when reading the voltage on the V_{BAT} and V_{DDA} input channels	5	-	-	μs

1. Guaranteed by design. Not tested in production.
2. Wait for the startup stabilization time t_{ADC_BUF} to enable the ADC internal V_{BAT} and V_{DDA} input channels. The sampling time for ADC to measure the voltage on the V_{BAT} and V_{DDA} input channels should be at least t_{SAMP}.

5.5.20 LCD controller characteristics

Table 5-34 LCD controller characteristics(1) (2)

Symbol	Description			Min	Typ	Max	Unit
V_{DD}	LCD supply voltage			1.8	-	5.5	V
$V_{LCD-PUMP}$	LCD voltage in charge pump mode		1/3bias	2.55	-	5.25	
			1/4bias	2.60	-	5.20	
$V_{LCD-RES}$	LCD voltage in on-chip resistor voltage division mode			0.548* V_{DD}	-	V_{DD}	
$V_{LCD-CAP}$	LCD voltage in off-chip capacitor voltage division mode			-	-	V_{DD}	
I_{LCD}	Charge pump mode	1/3bias V_{DD} = 3.3V	V_{LCD} = 5.25V	-	2.35	-	μA
			V_{LCD} = 2.55V	-	2.14	-	
		1/4bias V_{DD} = 3.3V	V_{LCD} = 5.20V	-	2.49	-	
			V_{LCD} = 2.60V	-	2.15	-	
	Internal resistor voltage division mode	V_{LCD} = V_{DD} = 3.3V	HD = 0	-	3.51	-	
			HD = 1	-	12.48	-	
		V_{LCD} = 0.548 *V_{DD} （V_{DD} = 3.3V）	HD = 1	-	6.84	-	
	External	V_{LCD} = V_{DD} = 3.3V		-	0.57	-	

Symbol	Description		Min	Typ	Max	Unit
	capacitor voltage division mode					
t_{STAB}(3)	Drive voltage stabilization time	V_{LCD} = 5.2V off-chip capacitance 0.1μF	-	82	100	ms

1. Derived from comprehensive assessment.
2. Unless otherwise specified, the configurations of the LCD controller are: 1/8 Duty, 1/4 bias, 32 Hz frame rate, charge pump clock frequency divider /16, full display for LCD_RAM, and no LCD display connection without a load.
3. When it is configured to the charge pump mode, after the LCD enable bit LCDEN is set to 1, wait for the drive voltage stabilization time t_{STAB} before setting the output control bit SCOC to 1, so as to output a stable display drive waveform.

5.5.21 64-level voltage division reference source characteristics

Table 5-35 64-level voltage division reference source characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
I_{DAC}	Power consumption	Input reference voltage source VREFBUF 3.0V	0.32	0.84	2.47	μA
t_{STAB}	Startup time	-	-	12	15.63	μs

1. Guaranteed by design. Not tested in production.

5.5.22 SPI characteristics

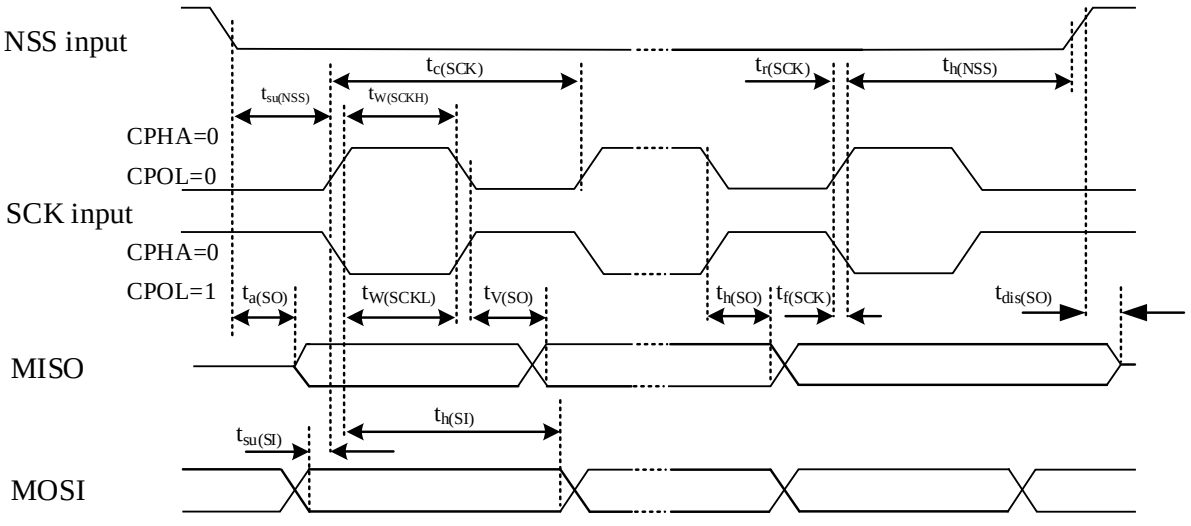
Table 5-36 SPI characteristics(1)

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode	-	-	20	MHz
		Slave mode	-	-	16	MHz
$t_{SU(NSS)}$	NSS setup time	Slave mode	4.35	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave	3.02	-	-	ns

Symbol	Description	Condition	Min	Typ	Max	Unit
		mode				
$t_{W(SCKH)}$	SCK high time	Master mode	$T_{SCK}/2-1$	$T_{SCK}/2$	$T_{SCK}/2+1$	ns
$t_{W(SCKL)}$	SCK low time	Master mode	$T_{SCK}/2-1$	$T_{SCK}/2$	$T_{SCK}/2+1$	ns
$t_{SU(MI)}$	Data input setup time	Master mode	-	-	3.18	ns
$t_{SU(SI)}$		Slave mode	1.98	-	-	ns
$t_{h(MI)}$	Data input hold time	Master mode	0	-	-	ns
$t_{h(SI)}$		Slave mode	9.7	-	-	ns
$t_{V(MO)}$	Data output valid time	Master mode	-	-	2.94	ns
$t_{V(SO)}$		Slave mode	-	-	29.30	ns
$t_{h(MO)}$	Data output hold time	Master mode	2.42	-	-	ns
$t_{h(SO)}$		Slave mode	22.38	-	-	ns

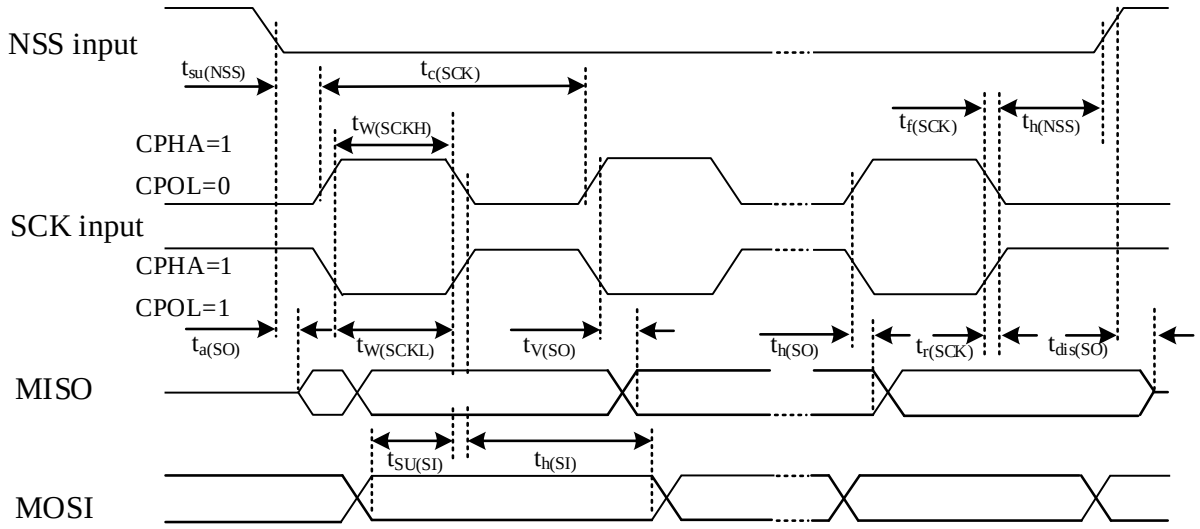
1. Guaranteed by design. Not tested in production.

Figure 5-2 SPI timing diagram - slave mode (CPHA = 0)(1)



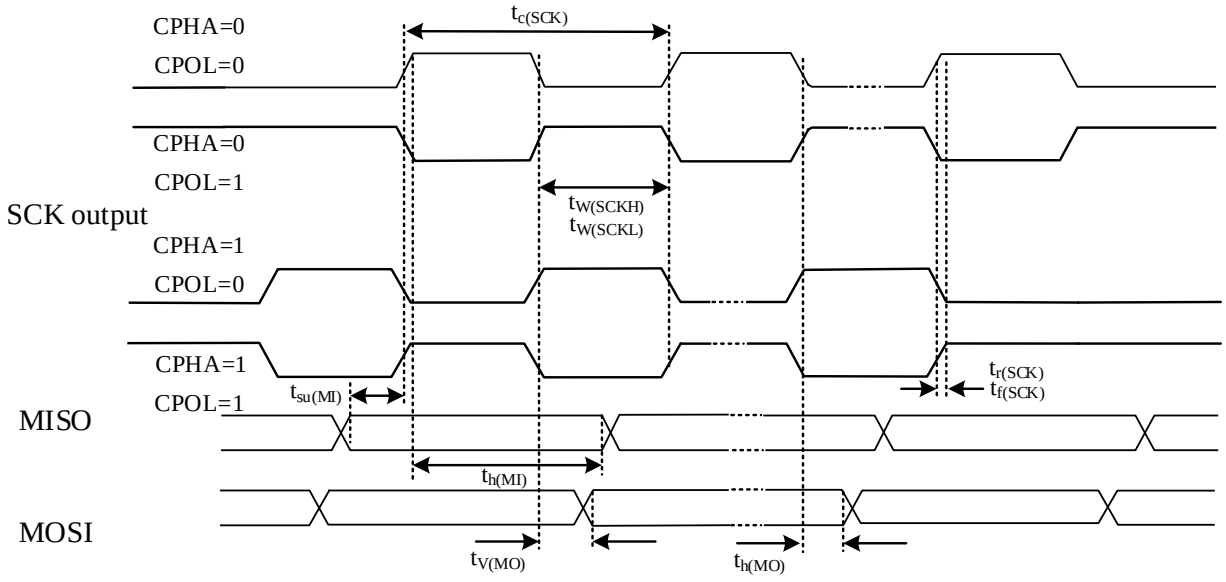
1. Measurement points are done at levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 5-3 SPI timing diagram - slave mode (CPHA = 1)(1)



1. Measurement points are done at levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 5-4 SPI timing diagram - master mode(1)



1. Measurement points are done at levels: $0.3V_{DD}$ and $0.7V_{DD}$.

6 Package information

CIU32L051 offers LQFP64(7 x 7 x 1.4 - 0.4mm), LQFP48(7 x 7 x 1.4 - 0.5mm), QFN32(4 x 4 x 0.75 - 0.4mm), SSOP24(8.65 x 3.90 x 1.40-0.635mm) and multiple packages. It complies with the JEDEC standard. The package dimension and size information are described in this chapter.

6.1 LQFP64 package information

Figure 6-1 LQFP64 (7 x 7 x 1.4 - 0.4mm) package outline

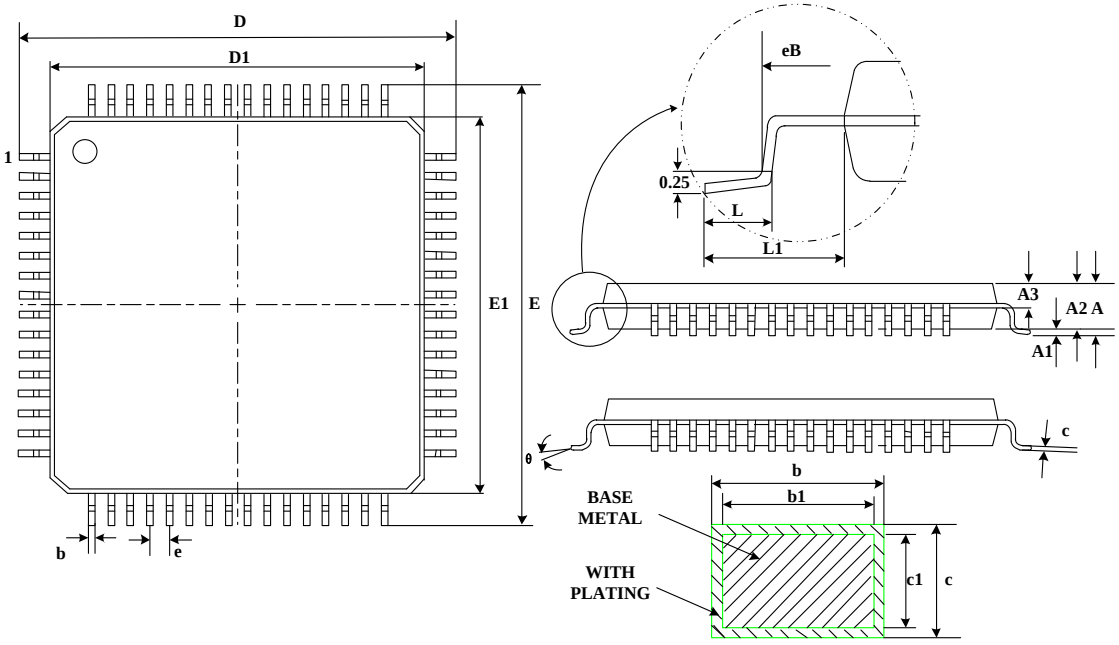


Table 6-1 LQFP64 (7 x 7 x 1.4 - 0.4mm) package outline dimension data

Symbol	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10

Symbol	Min	Typ	Max
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.40BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

6.2 LQFP48 package information

Figure 6-2 LQFP48 (7 x 7 x 1.4 - 0.5mm) package outline

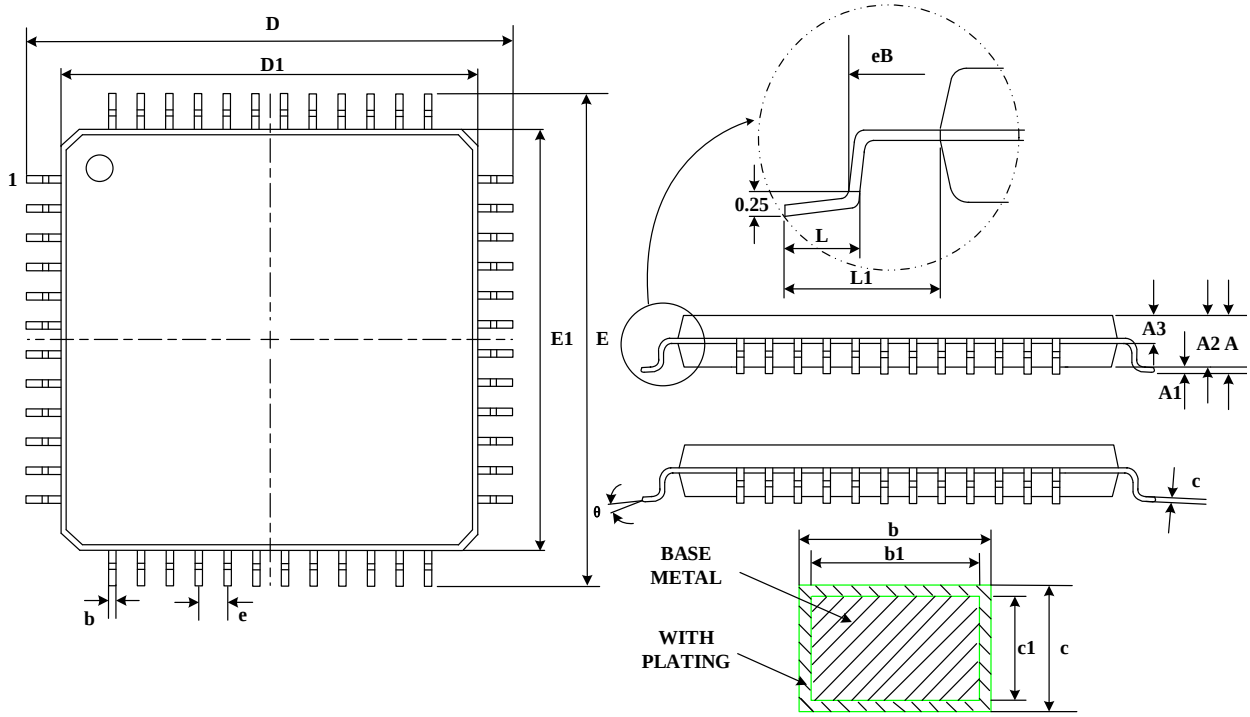


Table 6-2 LQFP48 (7 x 7 x 1.4 - 0.5mm) package outline dimension data

Symbol	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23

Symbol	Min	Typ	Max
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

6.3 QFN32 package information

Figure 6-3 QFN32 (4 x 4 x 0.75 - 0.4mm) package outline

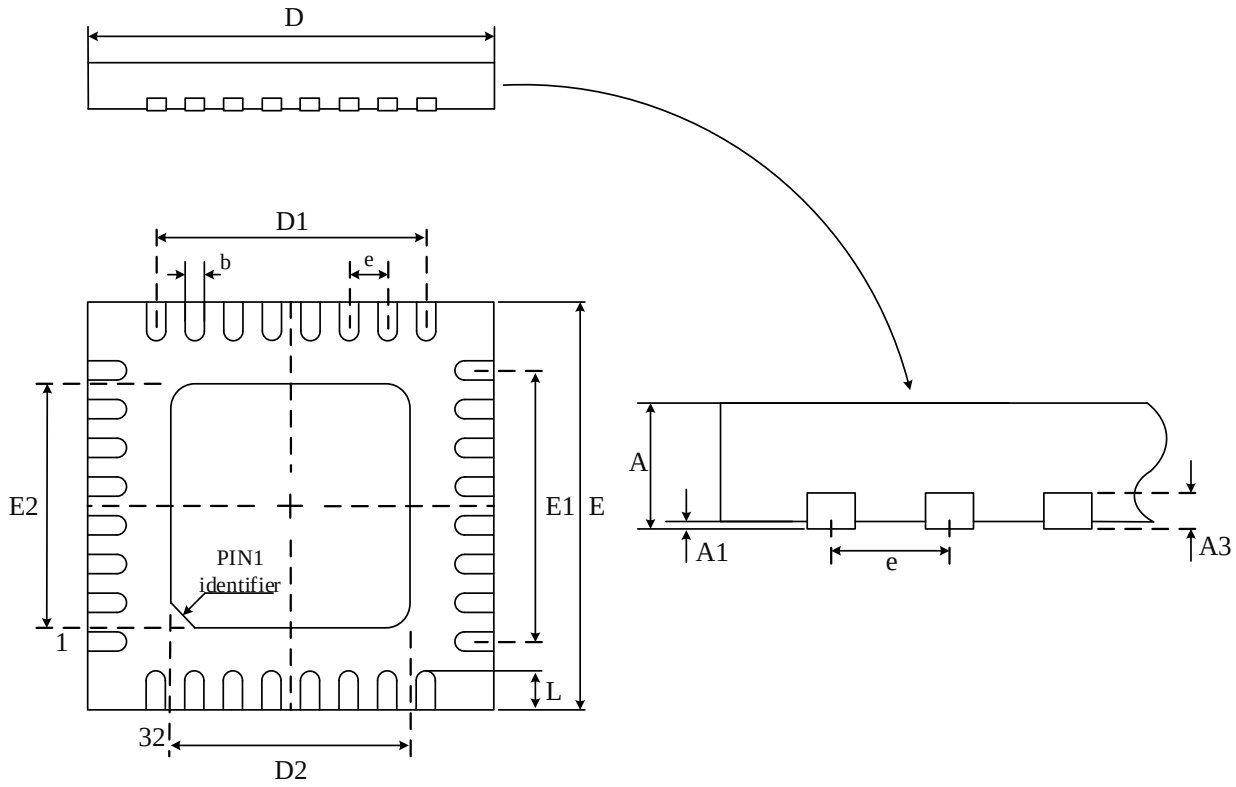


Table 6-3 QFN32 (4 x 4 x 0.75 - 0.4mm) package outline dimension data

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
A3	0.203REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D1	2.70	2.80	2.90
D2	2.55	2.65	2.80
E	3.90	4.00	4.10
E1	2.70	2.80	2.90
E2	2.55	2.65	2.80
e	0.40BSC		
L	0.35	0.40	0.45

6.4 SSOP24 package information

Figure 6-4 SSOP24 (8.65 x 3.90 x 1.40 - 0.635mm) package outline

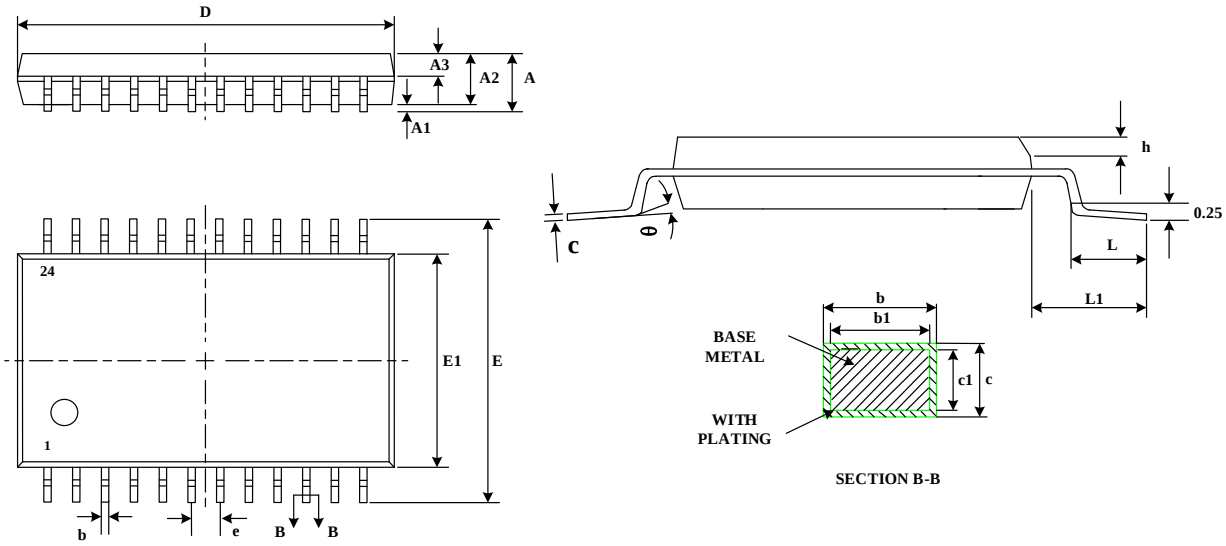


Table 6-4 SSOP24 (8.65 x 3.90 x 1.40 - 0.635mm) package outline dimension data

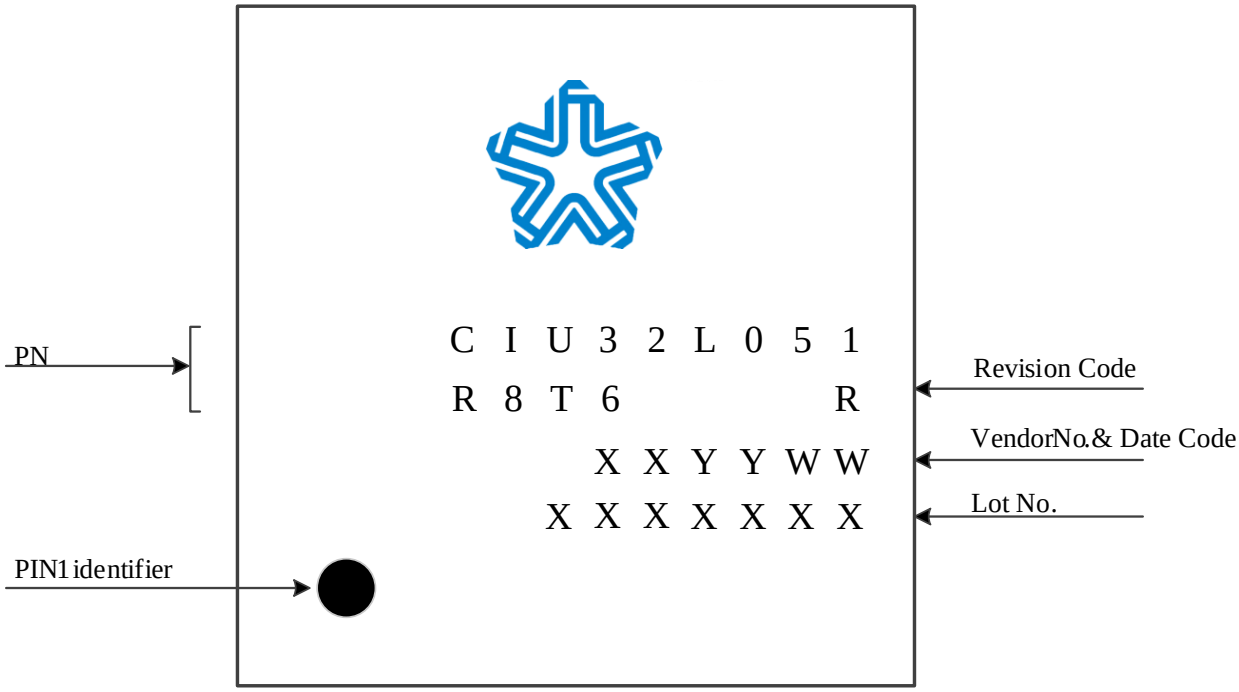
Symbol	Min	Typ	Max
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

6.5 Silk screen description

The PIN1 identifier location and topside marking information on each package for the CIU32L051 ultra-low-power security MCU are as follows:

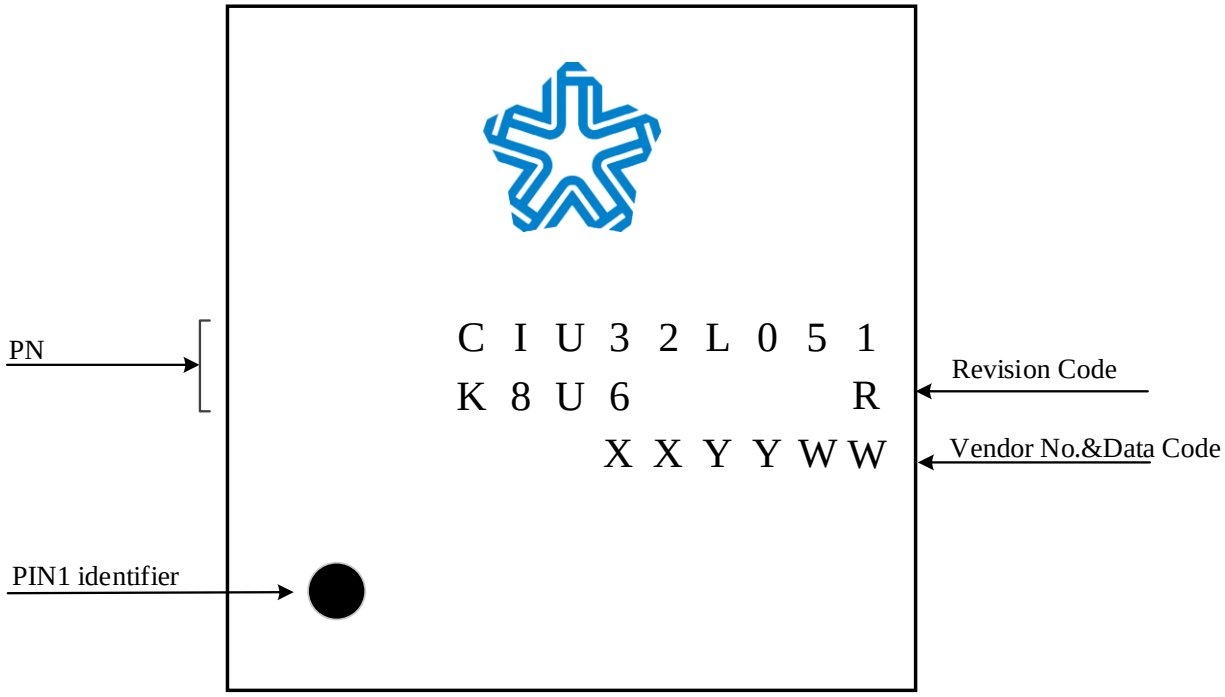
Silk screen for LQFP64 and LQFP48 packages

Figure 6-5 LQFP64 and LQFP48 silk screen information description



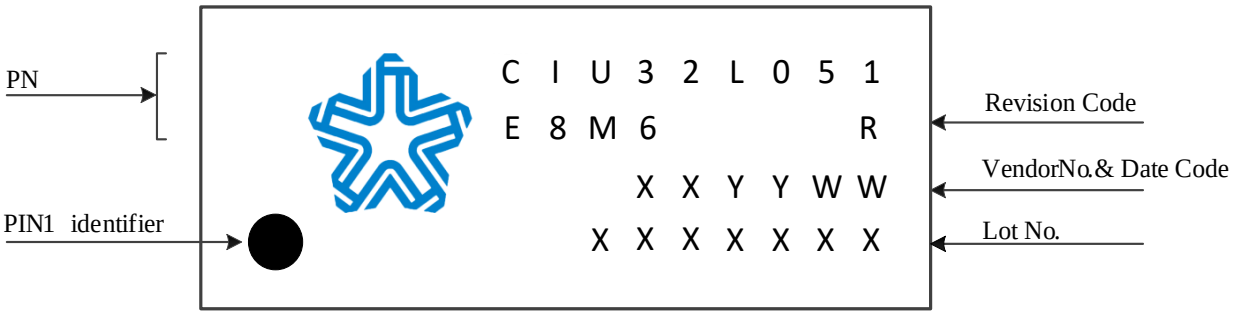
Silk screen for QFN32 package

Figure 6-6 QFN32 silk screen information description



Silk screen for QFN32 package

Figure 6-7 SSOP24 silk screen information description



7 Ordering information

CIU 32 L 0 51 R 8 T 6 xx

CPU bit width

32: 32bit

Product type

L: Ultra-low power consumption

Core

0: Cortex-M0+

Device subfamily

51: CIU32L051

Pin count

E: 24Pin
K: 32Pin
C: 48Pin
R: 64Pin

Flash memory size

8: 64K

Package type

T: LQFP
U: QFN
M: SSOP

Temperature range

6: -40 ~ 85℃

Packing form

TR: Reel
TY: Pallet
TU: Tube

8 Revision history

Table 8-1 Revision history

Date	Revision	Changes
2023-11-15	V1.0	Initial release.
2024-4-7	V1.1	1. Added relevant content in SSOP24 package. 2. Corrected relevant content in electrical characteristics.
2024-4-28	V1.2	Corrected relevant content in 5.5.5 Supply current characteristics.
2024-5-16	V1.3	Corrected relevant content in 5.5.10 Flash memory characteristics.
2024-11-5	V1.4	Added the circuitry of typical applications, there are some considerations: In VBAT mode, the VBAT_MODE_EN bit should be configured to 1; In other mode, the VBAT_MODE_EN bit configured should be configured to 0.
2024-12-3	V1.5	1. Corrected relevant content in 5.5.10 Flash memory characteristics. 2. Corrected relevant content in 5.5.20 LCD controller characteristics.
2024-12-30	V1.6	Corrected relevant content in 6.3 QFN32 package
2025-1-13	V1.7	1. Corrected relevant content in 5.5.4 Embedded voltage reference. 2. Corrected relevant content in 5.5.10 Flash memory characteristics. 3. Corrected relevant content in 5.5.16 VREFBUF characteristics.
2025-2-8	V1.8	Corrected relevant content in 5.5.5 Supply current characteristics.

9 Contact information

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Feel free to contact us for any comment or suggestion during purchase and use.